GC9D01N

a-Si TFT LCD Single Chip Driver
160RGBx160 Resolution

Datasheet

V1.1

2021-04-09

Ordering Information

◆ **GC9D01N**

(a-Si TFT LCD Single Chip Driver 160RGBx160 Resolution)

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Galaxycore Incorporation

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Introduction

GC9D01N is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 160RGBx160 dots, comprising a 240-channel source driver, a 32-channel gate driver, 57,600 bytes GRAM for graphic display data of 160RGBx160 dots, and power supply circuit.

GC9D01N supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface , 3-/4-line serial peripheral interface (SPI) , 3 line 2data lane interface and MIPI interface . The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

GC9D01N supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9D01N an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

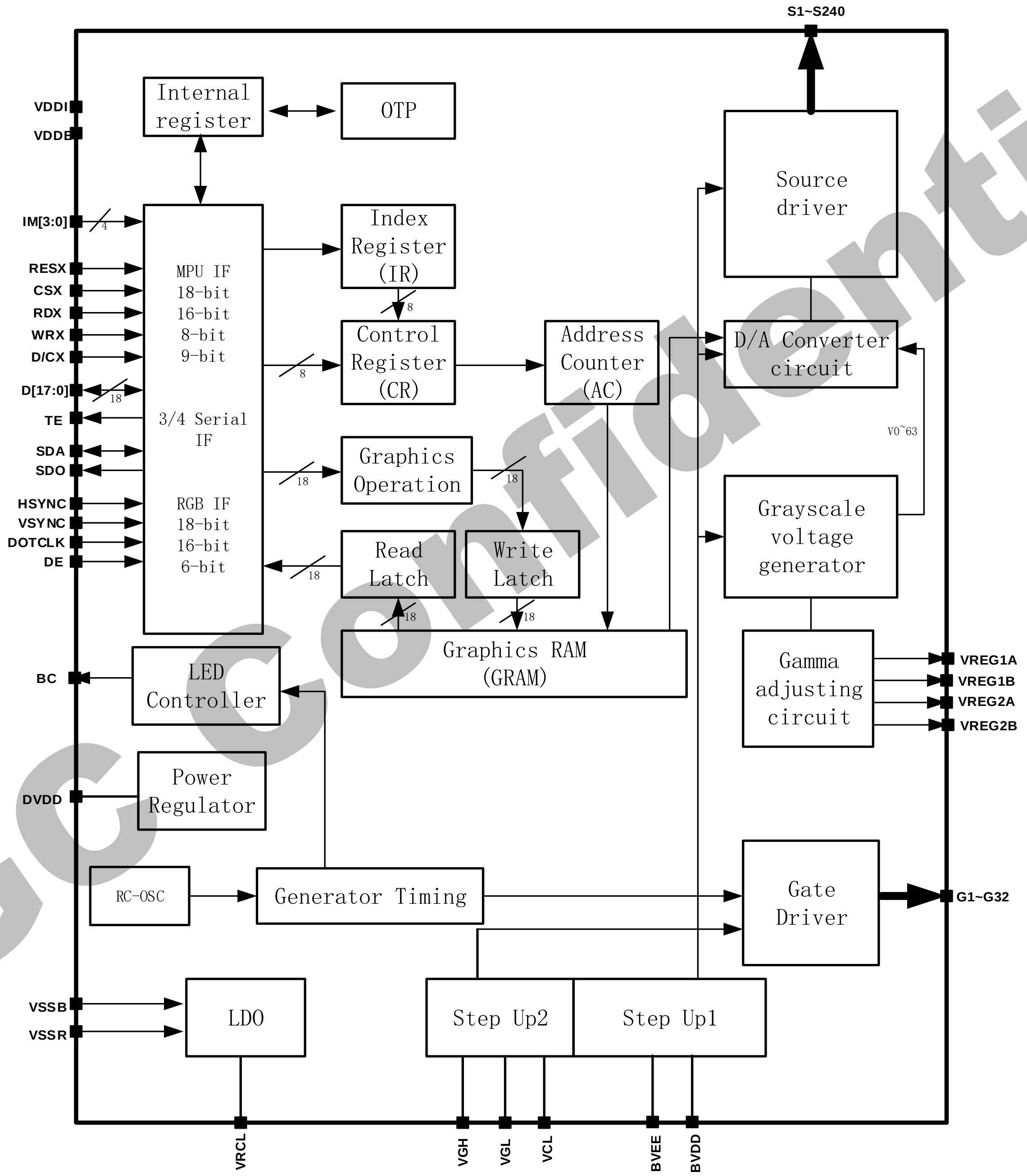
Features

- Dual gate and single gate TFT LCD driver with 0D 0C
- Display resolution: [160 RGB] (H) x 160(V)
- Output:
  - 240 source outputs
  - 32 gate outputs
- Resolution:
  160RGBx160：S1-S240　Dual gate（default）; 120RGBX160：S31-S210 Dual gate
  80RGBX160：S1-S240 Single gate;　　　　　40RGBX160：S61-S180 Single gate
- a-TFT LCD driver with on-chip full display RAM: 57,600 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-I /8080-II series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 8-bits, 9-bits Serial Peripheral Interface (SPI) and 2 data lane SPI
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- Frame rate
  - Normal mode（20Hz~65Hz）
  - Idle mode　（1Hz~30Hz）
- On chip functions:
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Dual Gate Support driving method 1+2H1V,1+2column,2column
  - Single Gate Support Column,1-dot
- Low -power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3V (logic)
    - VDDB = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/Gamma power supply voltage
    - VAP (GVDD) to VAN (GVCL): +6.4~-4.4V
  - Gate driver output voltage
    - VGH voltage range:9V~14V
    - VGL voltage range:-9V~-14 V
  - VCOM connect to GND
- Operate temperature range: -40℃to 85℃

1. Block Diagram

1.1. Block diagram

Figure1


S1~S240
VDDI
VDDB
IM[3:0]
4
RESX
CSX
RDX
WRX
D/CX
D[17:0]
18
TE
SDA
SDO
HSYNC
VSYNC
DOTCLK
DE
BC
DVDD
VSSB
VSSR
Internal register
OTP
MPU IF 18-bit 16-bit 8-bit 9-bit
3/4 Serial IF
RGB IF 18-bit 16-bit 6-bit
Index Register (IR)
8
Control Register (CR)
8
Address Counter (AC)
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18
18
Read Latch
Write Latch
18
18
18
Graphics RAM (GRAM)
Source driver
D/A Converter circuit
V0~63
Grayscale voltage generator
Gamma adjusting circuit
VREG1A
VREG1B
VREG2A
VREG2B
LED Controller
Power Regulator
RC-OSC
Generator Timing
Gate Driver
G1~G32
LDO
Step Up2
Step Up1
VRCL
VGH
VGL
VCL
BVEE
BVDD

1.2. Pin Description

Table 1.

Power Supply Pins			
Pin Name	I/O	Connect Pin	Descriptions
VDDI(IOVCC)	I	VDDI	Low voltage power supply for interface logic circuits(1.65~3.3V)
VDDB(VCI)	I	VDDB	High voltage power supply for analog circuit blocks(2.5~3.3V)
VSSB/VSSR	I	GND	System ground level

Table 2

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Connect Pin</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(VDDI/ GND)</td><td>-Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080- MCU 8bit interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080- MCU 9bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080-MCU16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10]
D[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8080- MCU 8bit interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>8080- MCU 9bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>8080- MCU 16bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8080- MCU 18bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td>SDA
SDO</td><td>SDA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface II</td><td>SDA
SDO</td><td>SDA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-wire 9-bit data serial interface I</td><td>SDA</td><td>SDA</td></tr>
<tr><td>2 data lane serial interface I</td><td>SDA</td><td>SDA/ D/CX</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface I</td><td>SDA</td><td>SDA</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.</td></tr>
</table>

			Fix this pin at VDDI or GND.
RESX	I	MCU (VDDI/GND)	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
CSX	I	MCU (VDDI/GND)	Chip select input pin("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only.
D/CX (SCL)	I	MCU (VDDI/ GND)	This pin is used to select "Data or Command" in the parallel interface When DCX='1', data is selected. When DCX='0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit /QSPI serial interface. If not used, this pin should be connected to VDDI or GND.
RDX	I	MCU (VDDI/ GND)	8080-I/8080-II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use
WRX (D/CX)	I	MCU (VDDI/ GND)	8080-I/8080-II system (WRX): Serves as a write signal and writes data at the rising edge. 4-wire system (D/CX): Serves as command or parameter select. 3-wire 2data mode：Serves as second data pin Fix to VDDI level when not in use.
D[17:0]	I/O	MCU (VDDI/ GND)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode QSPI 4wire mode D[3:1] Server as SDA[3:1] Fix to GND level when not in use
SDA	I/O	MCU (VDDI/ GND)	When IM[2]: High, Serial in/out signal in 3-wire 9-bit/4-wire 8-bit serial data interface. When IM[2]: Low, Serial input signal in 3-wire 9-bit/4-wire 8-bit serial data interface. When IM[3:0]= 1100, Serial input signal in QSPI serial data interface. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or GND.
SDO	O	MCU (VDDI/GND)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/ GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (VDDI/GND)	Dot clock signal for RGB interface operation. Fix to VDDI or GND level when not in use.

VSYNC	I	MCU (VDDI/GND)	Frame synchronizing signal for RGB interface operation. Fix to VDDI or GND level when not in use.
HSYNC	I	MCU (VDDI/ GND)	Line synchronizing signal for RGB interface operation. Fix to VDDI or GND level when not in use.
DE	I	MCU (VDDI/ GND)	Data enable signal for RGB interface operation. Fix to VDDI or GND level when not in use.
VCOM	I	GND	Fix to GND

Note:

1. If CSX is connected to GND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Further more there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

Table 3

LCD Driver Input/Output Pins			
Pin Name	I/O	Connect Pin	Descriptions
S240~S1	O	LCD	Source output signals.
			Leave the pin to open when not in use.
G1~G32	O	LCD	Gate output signals.
			Leave the pin to open when not in use.
VCOM	O	GND	Connect to GND.
DVDD	O	Power	Regulated Low voltage level for interface circuits Don’t apply any external power to this pin
VRCL	O	Power	Power of VGH & VGL.
VGH	O	Power	Power supply for the gate driver (Positive).
VGL	O	Power	Power supply for the gate driver (Negative).
BVDD	O	Power	Analog power for Source
BVEE	O	Power	Analog power for Source
VREG1A	O	Ref	VREG1A is the highest positive grayscale reference voltage of source driver.
VREG1B	O	Ref	VREG1B is the lowest positive grayscale reference voltage of source driver. test by VREGP pin
VREG2B	O	Ref	VREG2B is the lowest negative grayscale reference voltage of source driver, test by VREGP pin
VREG2A	O	Ref	VREG2A is the highest negative grayscale reference voltage of source driver , test VREGN pin
BC	O	Dig IO	Output pin for PWM (Pulse width Modulation) signal of LED driving.
			If not used, open this pin.

Table 4

Test Pins			
Pin Name	I/O	Connect Pin	Descriptions
OSC_IN	I/O	Open	Test pin
OSC_TEST	I/O	Open	Test pin
VPP	I/O	Open	Test pin
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation , leave these pads open.

Liquid crystal power supply specifications Table

Table 5

No.	Item		Description
1	TFT Source Driver		support 160*RGB（max）
2	TFT Gate Driver		32 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S240	V0~V63 grayscales
		G1~G32	VGH-VGL
5	Input Voltage	VDDI	1.65~3.30V
		VDDB	2.50~3.30V
6	Liquid Crystal Drive Voltages	BVDD	4.5~6.8V
		BVEE	-4.7V~-2.5V
		VGH	9.0~14.0V
		VGL	-14.0~-9.0V
		VCL	-3.0~-1.5V
7	Internal Step-up Circuits	VGH	VDDB*5
		VGL	VDDB*-5
		VCL	VDDB*-1

1.3. PAD coordinates

Pad No.	Text Name	X-axis	Y-axis	Pad No.	Text Name	X-axis	Y-axis
1	VCOM	-2998.01	-382	51	BC	-475.53	-382
2	VCOM	-2948.01	-382	52	TE	-421.43	-382
3	VCOM	-2898.01	-382	53	DB<17>	-357.845	-382
4	VGL	-2848.01	-382	54	DB<16>	-285.845	-382
5	VGL	-2798.01	-382	55	DB<15>	-213.845	-382
6	VGL	-2748.01	-382	56	DB<14>	-141.845	-382
7	VCL	-2698.01	-382	57	DB<13>	55.875	-382
8	VRCL	-2648.01	-382	58	DB<12>	127.875	-382
9	VGH	-2598.01	-382	59	DB<11>	199.875	-382
10	VGH	-2548.01	-382	60	DB<10>	271.875	-382
11	VGH	-2498.01	-382	61	DB<9>	343.875	-382
12	VDDB	-2448.01	-382	62	DB<8>	415.875	-382
13	VDDB	-2398.01	-382	63	DB<7>	550.835	-382
14	VDDB	-2348.01	-382	64	DB<6>	622.835	-382
15	VDDB	-2298.01	-382	65	DB<5>	694.835	-382
16	VSSB	-2248.01	-382	66	DB<4>	766.835	-382
17	VSSB	-2198.01	-382	67	DB<3>	838.835	-382
18	VSSB	-2148.01	-382	68	DB<2>	910.835	-382
19	VSSB	-2098.01	-382	69	DB<1>	982.835	-382
20	TESTN	-2048.01	-382	70	DB<0>	1054.835	-382
21	VREGN	-1998.01	-382	71	WRX	1119.815	-382
22	BVEE	-1948.01	-382	72	CSX	1177.775	-382
23	BVEE	-1898.01	-382	73	DCX	1235.735	-382
24	BVDD	-1848.01	-382	74	RDX	1293.695	-382
25	BVDD	-1798.01	-382	75	SDO	1356.55	-382
26	VREG1A	-1748.01	-382	76	SDA	1419.05	-382
27	VREGP	-1698.01	-382	77	RESX	1480.405	-382
28	VREG_VREF	-1648.01	-382	78	VPP	1530.405	-382
29	TESTP	-1598.01	-382	79	VSSB	1580.405	-382
30	VSSR	-1548.01	-382	80	VSSB	1630.405	-382
31	VSSR	-1498.01	-382	81	VSSB	1680.405	-382
32	VSSR	-1448.01	-382	82	IM<0>	1730.405	-382
33	VSSR	-1398.01	-382	83	IM<1>	1780.405	-382
34	VSSB	-1348.01	-382	84	IM<2>	1830.405	-382
35	VSSB	-1298.01	-382	85	IM<3>	1880.405	-382
36	VSSB	-1248.01	-382	86	VDDI	1930.405	-382
37	VSSB	-1198.01	-382	87	VDDI	1980.405	-382
38	DVDD	-1148.01	-382	88	VDDI	2030.405	-382
39	VDDB	-1098.01	-382	89	VDDI	2080.405	-382
40	VDDB	-1048.01	-382	90	VDDI	2130.405	-382
41	VDDB	-998.01	-382	91	VDDB	2180.405	-382
42	VDDB	-948.01	-382	92	VDDB	2230.405	-382
43	VDDI	-898.01	-382	93	VDDB	2280.405	-382
44	VDDI	-848.01	-382	94	VDDB	2330.405	-382
45	OSC_TEST	-798.01	-382	95	VDDB	2380.405	-382
46	OSC_IN	-748.01	-382	96	VSSB	2430.405	-382
47	DOTCLK	-691.93	-382	97	VSSB	2480.405	-382
48	ENABLE	-637.83	-382	98	VSSB	2530.405	-382
49	VSYNC	-583.73	-382	99	VSSB	2580.405	-382
50	HSYNC	-529.63	-382	100	VSSB	2630.405	-382

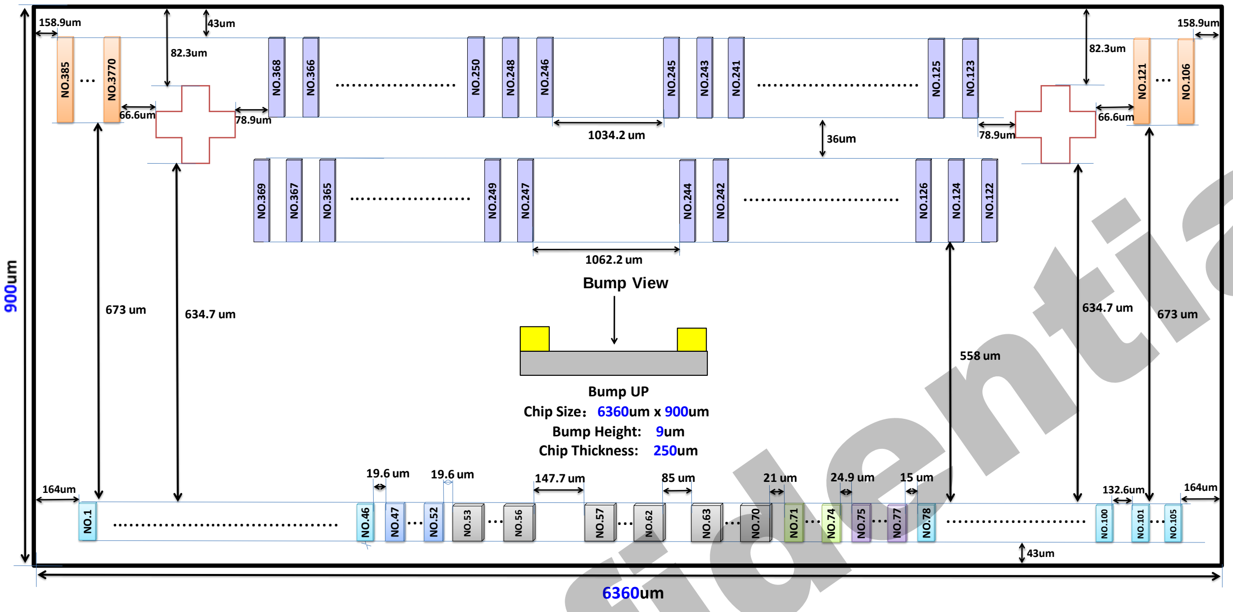
Pad No.	Text Name	X-axis	Y-axis	Pad No.	Text Name	X-axis	Y-axis
101	VCOM	2798.01	-382	151	S<28>	1839.3	364.5
102	VCOM	2848.01	-382	152	S<29>	1825.305	243.5
103	VCOM	2898.01	-382	153	S<30>	1811.305	364.5
104	VCOM	2948.01	-382	154	S<31>	1797.31	243.5
105	VCOM	2998.01	-382	155	S<32>	1783.31	364.5
106	GOUT<32>	3011.535	361.5	156	S<33>	1769.315	243.5
107	GOUT<31>	2976.255	361.5	157	S<34>	1755.315	364.5
108	GOUT<30>	2940.975	361.5	158	S<35>	1741.32	243.5
109	GOUT<29>	2905.695	361.5	159	S<36>	1727.32	364.5
110	GOUT<28>	2870.415	361.5	160	S<37>	1713.325	243.5
111	GOUT<27>	2835.135	361.5	161	S<38>	1699.325	364.5
112	GOUT<26>	2799.855	361.5	162	S<39>	1685.33	243.5
113	GOUT<25>	2764.575	361.5	163	S<40>	1671.33	364.5
114	GOUT<24>	2729.295	361.5	164	S<41>	1657.335	243.5
115	GOUT<23>	2694.015	361.5	165	S<42>	1643.335	364.5
116	GOUT<22>	2658.735	361.5	166	S<43>	1629.34	243.5
117	GOUT<21>	2623.455	361.5	167	S<44>	1615.34	364.5
118	GOUT<20>	2588.175	361.5	168	S<45>	1601.345	243.5
119	GOUT<19>	2552.895	361.5	169	S<46>	1587.345	364.5
120	GOUT<18>	2517.615	361.5	170	S<47>	1573.35	243.5
121	GOUT<17>	2482.335	361.5	171	S<48>	1559.35	364.5
122	DUM	2245.23	243.5	172	S<49>	1545.355	243.5
123	DUM	2231.23	364.5	173	S<50>	1531.355	364.5
124	S<1>	2217.235	243.5	174	S<51>	1517.36	243.5
125	S<2>	2203.235	364.5	175	S<52>	1503.36	364.5
126	S<3>	2189.24	243.5	176	S<53>	1489.365	243.5
127	S<4>	2175.24	364.5	177	S<54>	1475.365	364.5
128	S<5>	2161.245	243.5	178	S<55>	1461.37	243.5
129	S<6>	2147.245	364.5	179	S<56>	1447.37	364.5
130	S<7>	2133.25	243.5	180	S<57>	1433.375	243.5
131	S<8>	2119.25	364.5	181	S<58>	1419.375	364.5
132	S<9>	2105.255	243.5	182	S<59>	1405.38	243.5
133	S<10>	2091.255	364.5	183	S<60>	1391.38	364.5
134	S<11>	2077.26	243.5	184	S<61>	1377.385	243.5
135	S<12>	2063.26	364.5	185	S<62>	1363.385	364.5
136	S<13>	2049.265	243.5	186	S<63>	1349.39	243.5
137	S<14>	2035.265	364.5	187	S<64>	1335.39	364.5
138	S<15>	2021.27	243.5	188	S<65>	1321.395	243.5
139	S<16>	2007.27	364.5	189	S<66>	1307.395	364.5
140	S<17>	1993.275	243.5	190	S<67>	1293.4	243.5
141	S<18>	1979.275	364.5	191	S<68>	1279.4	364.5
142	S<19>	1965.28	243.5	192	S<69>	1265.405	243.5
143	S<20>	1951.28	364.5	193	S<70>	1251.405	364.5
144	S<21>	1937.285	243.5	194	S<71>	1237.41	243.5
145	S<22>	1923.285	364.5	195	S<72>	1223.41	364.5
146	S<23>	1909.29	243.5	196	S<73>	1209.415	243.5
147	S<24>	1895.29	364.5	197	S<74>	1195.415	364.5
148	S<25>	1881.295	243.5	198	S<75>	1181.42	243.5
149	S<26>	1867.295	364.5	199	S<76>	1167.42	364.5
150	S<27>	1853.3	243.5	200	S<77>	1153.425	243.5

Pad No.	Text Name	X-axis	Y-axis	Pad No.	Text Name	X-axis	Y-axis
201	S<78>	1139.425	364.5	251	S<124>	-593.525	243.5
202	S<79>	1125.43	243.5	252	S<125>	-607.52	364.5
203	S<80>	1111.43	364.5	253	S<126>	-621.52	243.5
204	S<81>	1097.435	243.5	254	S<127>	-635.515	364.5
205	S<82>	1083.435	364.5	255	S<128>	-649.515	243.5
206	S<83>	1069.44	243.5	256	S<129>	-663.51	364.5
207	S<84>	1055.44	364.5	257	S<130>	-677.51	243.5
208	S<85>	1041.445	243.5	258	S<131>	-691.505	364.5
209	S<86>	1027.445	364.5	259	S<132>	-705.505	243.5
210	S<87>	1013.45	243.5	260	S<133>	-719.5	364.5
211	S<88>	999.45	364.5	261	S<134>	-733.5	243.5
212	S<89>	985.455	243.5	262	S<135>	-747.495	364.5
213	S<90>	971.455	364.5	263	S<136>	-761.495	243.5
214	S<91>	957.46	243.5	264	S<137>	-775.49	364.5
215	S<92>	943.46	364.5	265	S<138>	-789.49	243.5
216	S<93>	929.465	243.5	266	S<139>	-803.485	364.5
217	S<94>	915.465	364.5	267	S<140>	-817.485	243.5
218	S<95>	901.47	243.5	268	S<141>	-831.48	364.5
219	S<96>	887.47	364.5	269	S<142>	-845.48	243.5
220	S<97>	873.475	243.5	270	S<143>	-859.475	364.5
221	S<98>	859.475	364.5	271	S<144>	-873.475	243.5
222	S<99>	845.48	243.5	272	S<145>	-887.47	364.5
223	S<100>	831.48	364.5	273	S<146>	-901.47	243.5
224	S<101>	817.485	243.5	274	S<147>	-915.465	364.5
225	S<102>	803.485	364.5	275	S<148>	-929.465	243.5
226	S<103>	789.49	243.5	276	S<149>	-943.46	364.5
227	S<104>	775.49	364.5	277	S<150>	-957.46	243.5
228	S<105>	761.495	243.5	278	S<151>	-971.455	364.5
229	S<106>	747.495	364.5	279	S<152>	-985.455	243.5
230	S<107>	733.5	243.5	280	S<153>	-999.45	364.5
231	S<108>	719.5	364.5	281	S<154>	-1013.45	243.5
232	S<109>	705.505	243.5	282	S<155>	-1027.445	364.5
233	S<110>	691.505	364.5	283	S<156>	-1041.445	243.5
234	S<111>	677.51	243.5	284	S<157>	-1055.44	364.5
235	S<112>	663.51	364.5	285	S<158>	-1069.44	243.5
236	S<113>	649.515	243.5	286	S<159>	-1083.435	364.5
237	S<114>	635.515	364.5	287	S<160>	-1097.435	243.5
238	S<115>	621.52	243.5	288	S<161>	-1111.43	364.5
239	S<116>	607.52	364.5	289	S<162>	-1125.43	243.5
240	S<117>	593.525	243.5	290	S<163>	-1139.425	364.5
241	S<118>	579.525	364.5	291	S<164>	-1153.425	243.5
242	S<119>	565.53	243.5	292	S<165>	-1167.42	364.5
243	S<120>	551.53	364.5	293	S<166>	-1181.42	243.5
244	DUM	537.535	243.5	294	S<167>	-1195.415	364.5
245	DUM	523.535	364.5	295	S<168>	-1209.415	243.5
246	DUM	-523.535	364.5	296	S<169>	-1223.41	364.5
247	DUM	-537.535	243.5	297	S<170>	-1237.41	243.5
248	S<121>	-551.53	364.5	298	S<171>	-1251.405	364.5
249	S<122>	-565.53	243.5	299	S<172>	-1265.405	243.5
250	S<123>	-579.525	364.5	300	S<173>	-1279.4	364.5

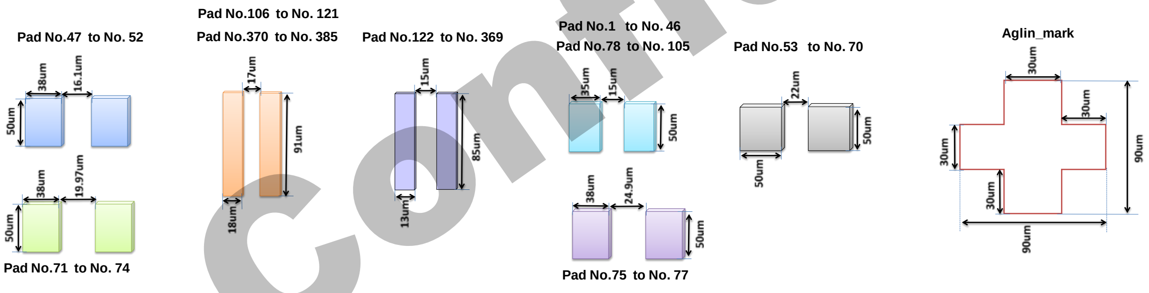
Pad No.	Text Name	X-axis	Y-axis	Pad No.	Text Name	X-axis	Y-axis
301	S<174>	-1293.4	243.5	351	S<224>	-1993.275	243.5
302	S<175>	-1307.395	364.5	352	S<225>	-2007.27	364.5
303	S<176>	-1321.395	243.5	353	S<226>	-2021.27	243.5
304	S<177>	-1335.39	364.5	354	S<227>	-2035.265	364.5
305	S<178>	-1349.39	243.5	355	S<228>	-2049.265	243.5
306	S<179>	-1363.385	364.5	356	S<229>	-2063.26	364.5
307	S<180>	-1377.385	243.5	357	S<230>	-2077.26	243.5
308	S<181>	-1391.38	364.5	358	S<231>	-2091.255	364.5
309	S<182>	-1405.38	243.5	359	S<232>	-2105.255	243.5
310	S<183>	-1419.375	364.5	360	S<233>	-2119.25	364.5
311	S<184>	-1433.375	243.5	361	S<234>	-2133.25	243.5
312	S<185>	-1447.37	364.5	362	S<235>	-2147.245	364.5
313	S<186>	-1461.37	243.5	363	S<236>	-2161.245	243.5
314	S<187>	-1475.365	364.5	364	S<237>	-2175.24	364.5
315	S<188>	-1489.365	243.5	365	S<238>	-2189.24	243.5
316	S<189>	-1503.36	364.5	366	S<239>	-2203.235	364.5
317	S<190>	-1517.36	243.5	367	S<240>	-2217.235	243.5
318	S<191>	-1531.355	364.5	368	DUM	-2231.23	364.5
319	S<192>	-1545.355	243.5	369	DUM	-2245.23	243.5
320	S<193>	-1559.35	364.5	370	GOUT<16>	-2482.335	361.5
321	S<194>	-1573.35	243.5	371	GOUT<15>	-2517.615	361.5
322	S<195>	-1587.345	364.5	372	GOUT<14>	-2552.895	361.5
323	S<196>	-1601.345	243.5	373	GOUT<13>	-2588.175	361.5
324	S<197>	-1615.34	364.5	374	GOUT<12>	-2623.455	361.5
325	S<198>	-1629.34	243.5	375	GOUT<11>	-2658.735	361.5
326	S<199>	-1643.335	364.5	376	GOUT<10>	-2694.015	361.5
327	S<200>	-1657.335	243.5	377	GOUT<9>	-2729.295	361.5
328	S<201>	-1671.33	364.5	378	GOUT<8>	-2764.575	361.5
329	S<202>	-1685.33	243.5	379	GOUT<7>	-2799.855	361.5
330	S<203>	-1699.325	364.5	380	GOUT<6>	-2835.135	361.5
331	S<204>	-1713.325	243.5	381	GOUT<5>	-2870.415	361.5
332	S<205>	-1727.32	364.5	382	GOUT<4>	-2905.695	361.5
333	S<206>	-1741.32	243.5	383	GOUT<3>	-2940.975	361.5
334	S<207>	-1755.315	364.5	384	GOUT<2>	-2976.255	361.5
335	S<208>	-1769.315	243.5	385	GOUT<1>	-3011.535	361.5
336	S<209>	-1783.31	364.5				
337	S<210>	-1797.31	243.5				
338	S<211>	-1811.305	364.5				
339	S<212>	-1825.305	243.5				
340	S<213>	-1839.3	364.5				
341	S<214>	-1853.3	243.5				
342	S<215>	-1867.295	364.5				
343	S<216>	-1881.295	243.5				
344	S<217>	-1895.29	364.5				
345	S<218>	-1909.29	243.5				
346	S<219>	-1923.285	364.5				
347	S<220>	-1937.285	243.5				
348	S<221>	-1951.28	364.5				
349	S<222>	-1965.28	243.5				
350	S<223>	-1979.275	364.5				

Name	X-axis	Y-axis
left mark	-2361.965	322.7
right mark	2361.965	322.7

Chip Size (include scribe line): 6360um x 900um	
Chip thickness: 250um	
Bump height: 9um	



158.9um
43um
82.3um
NO.385
NO.3770
66.6um
78.9um
NO.368
NO.366
NO.250
NO.248
NO.246
NO.245
NO.243
NO.241
NO.125
NO.123
NO.121
NO.106
158.9um
82.3um
66.6um
78.9um
1034.2 um
36um
NO.369
NO.367
NO.365
NO.249
NO.247
NO.244
NO.242
NO.126
NO.124
NO.122
1062.2 um
900um
673 um
634.7 um
Bump View
634.7 um
673 um
558 um
Bump UP
Chip Size：6360um x 900um
Bump Height: 9um
Chip Thickness: 250um
164um
19.6 um
19.6 um
147.7 um
85 um
21 um
24.9 um
15 um
132.6um
164um
NO.1
NO.46
NO.47
NO.52
NO.53
NO.56
NO.57
NO.62
NO.63
NO.70
NO.71
NO.74
NO.75
NO.77
NO.78
NO.100
NO.101
NO.105
43um
6360um



Pad No.47 to No. 52
38um
16.1um
50um
38um
19.97um
50um
Pad No.71 to No. 74
Pad No.106 to No. 121
Pad No.370 to No. 385
17um
91um
18um
Pad No.122 to No. 369
15um
85um
13um
Pad No.1 to No. 46
Pad No.78 to No. 105
35um
15um
50um
38um
24.9um
50um
Pad No.75 to No. 77
Pad No.53 to No. 70
22um
50um
50um
Aglin_mark
30um
30um
30um
30um
90um
90um

2. Interface setting

2.1. MCU interfaces

GC9D01N provides the 8-/9-/16-/18-bit parallel system interface for 8080-Ⅰ/8080- Ⅱ series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] 3-bits of 3Ah register.

2.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

Table 6

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080- MCU 8bit bus interface II	D[7:10]	D[17:10] ,WRX,RDX,CSX,D/CX
0	0	0	1	8080- MCU 9bit bus interface II	D[7:10]	D[17: 9],WRX,RDX,CSX,D/CX
0	0	1	0	8080- MCU 16bit bus interface II	D[8: 1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
0	0	1	1	8080- MCU 18bit bus interface II	D[8: 1]	D[17: 0], WRX,RDX,CSX,D/CX
0	1	0	0	8080- MCU 8bit bus interface I	D[7: 0]	D[7: 0] , WRX,RDX,CSX,D/CX
0	1	0	1	8080- MCU 9bit bus interface I	D[7: 0]	D[8: 0] , WRX,RDX,CSX,D/CX
0	1	1	0	8080- MCU 16bit bus interface I	D[7: 0]	D[15: 0] , WRX,RDX,CSX,D/CX
0	1	1	1	8080- MCU 18bit bus interface I	D[7: 0]	D[17: 0] , WRX,RDX,CSX,D/CX
1	0	0	0	X	X	X
1	0	0	1	3-wire 9-bit data serial interface II	SDA/SDO	SCL, SDA, CSX
1	0	1	0	X	X	X
1	0	1	1	4-wire 8-bit data serial interface II	SDA/SDO	SCL, SDA, D/CX, CSX
1	1	0	0	X	X	X
1	1	0	1	3-wire 9-bit data serial interface I	SDA	SCL, SDA, CSX
				2data lane serial interface I	SDA	SCL, SDA, CSX,D/CX
1	1	1	0	X	X	X
1	1	1	1	4-wire 8-bit data serial interface I	SDA	SCL, SDA, D/CX, CSX

2.1.2. 8080-I Series Parallel Interface

GC9D01N can be accessed via 8-/9-/16-/18-bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable GC9D01N chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9D01N latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The selection of 8080-I series parallel interface is shown as the table in the following.

Table 7

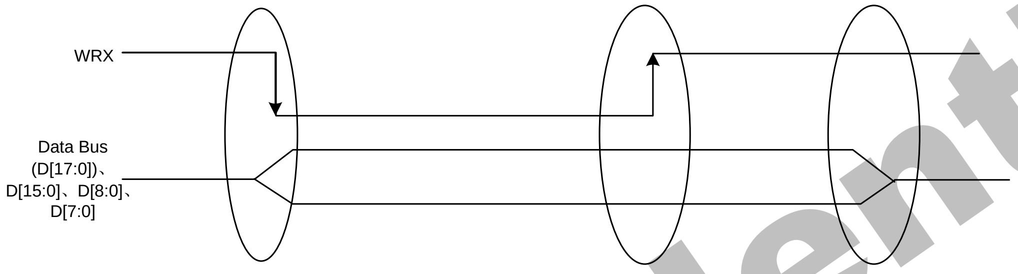
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	1	0	0	8080 MCU 8-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
0	1	1	0	8080 MCU 16-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
0	1	0	1	8080 MCU 9-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
0	1	1	1	8080 MCU 18-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.

2.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is SRAM data or command’s parameter.

The following figure shows a write cycle for the 8080-I MCU interface.

Figure 2.


WRX
Data Bus (D[17:0])、D[15:0]、D[8:0]、D[7:0]

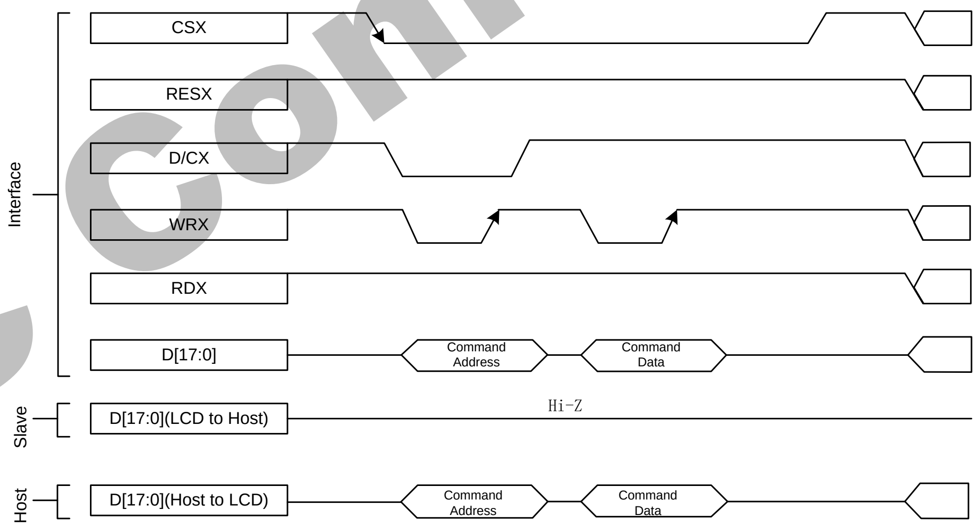
The host asserts D[17:0]、D[15:0]、 D[8:0] or D[7:0] lines when there is falling edge of WRX

The slave reads D[17:0]、D[15:0]、D[8:0] or D[7:0] lines when there is rising edge of WRX

The host negates D[17:0]、D[15:0]、D[8:0] or D[7:0] lines

Note: WRX is an unsynchronized signal (It can be stopped)

Figure 3.


CSX
RESX
D/CX
WRX
RDX
D[17:0]
Command Address
Command Data
Interface
Slave
D[17:0](LCD to Host)
Hi-Z
Host
D[17:0](Host to LCD)
Command Address
Command Data

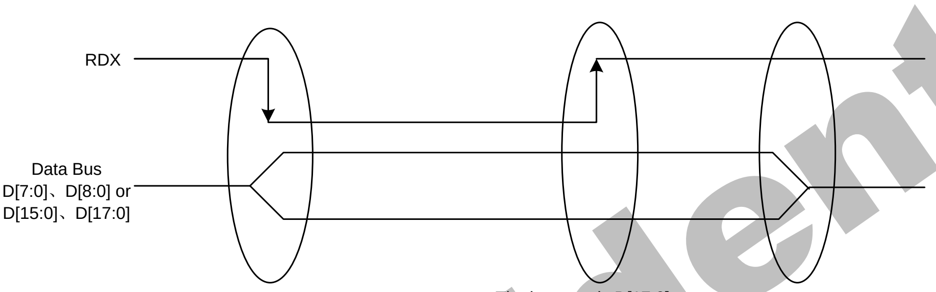
Signals on D[17:0],D/CX,RDX and WRX wires during CSX=” H” are ignored

2.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-I MCU interface.

Figure 4.


RDX
Data Bus
D[7:0]、D[8:0] or
D[15:0]、D[17:0]

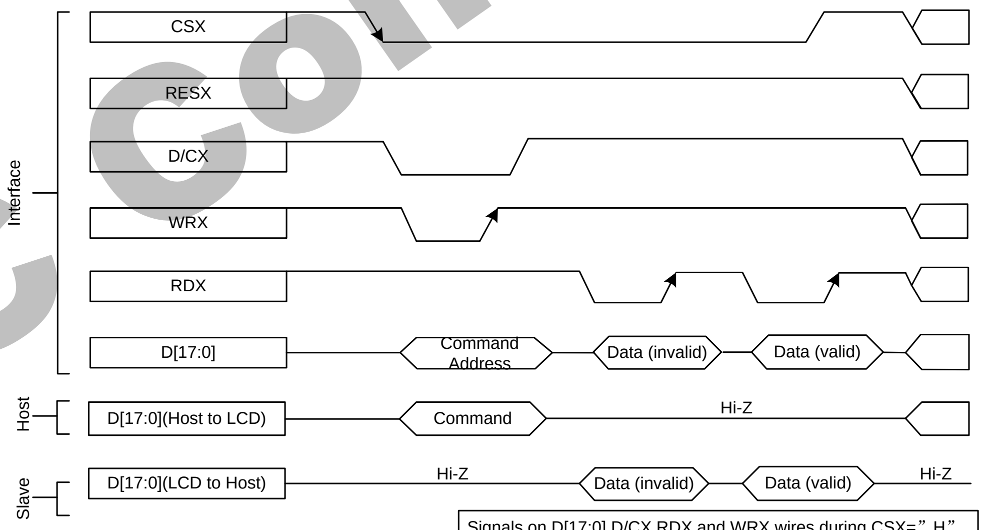
The slave assers D[17:0]、D[15:0]、D[8:0] or D[7:0] lines when there is a falling edge of RDX

The host reads D[17:0] 、D[15:0]、D[8:0] or D[7:0] lines when there is a rising edge of RDX

The slave negates D[17:0] 、D[15:0]、D[8:0] or D[7:0] lines

Note: RDX is an unsynchronized signal (It can be stopped).

Figure 5.


Interface
CSX
RESX
D/CX
WRX
RDX
D[17:0]
Command Address
Data (invalid)
Data (valid)
Host
D[17:0](Host to LCD)
Command
Hi-Z
Slave
D[17:0](LCD to Host)
Hi-Z
Data (invalid)
Data (valid)
Hi-Z

Signals on D[17:0],D/CX,RDX and WRX wires during CSX=”H” are ignored

Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

2.1.5. 8080-Ⅱ Series Parallel Interface

GC9D01N can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip select CSX (active low) is used to enable or disable GC9D01N chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9D01N latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.
The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip.
The selection of 8080-II series parallel interface is shown as the table in the following.

Table 8

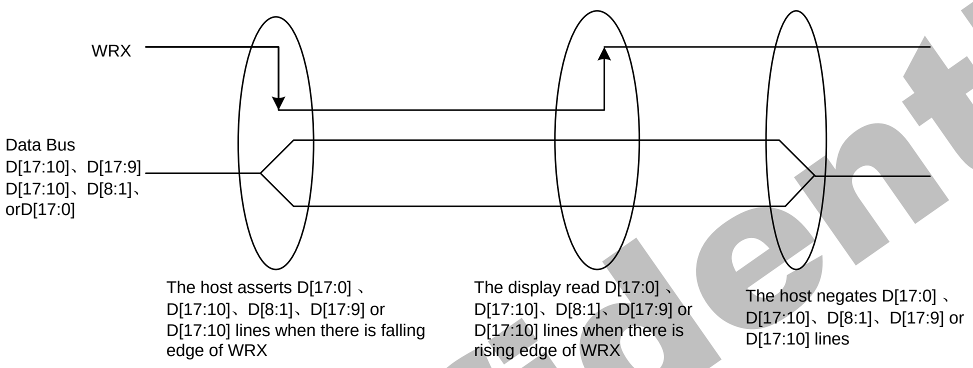
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	0	1	0	8080 MCU 16-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	0	8080 MCU 8-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 9-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

2.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-II MCU interface.

Figure 6.


WRX
Data Bus
D[17:10]、D[17:9]
D[17:10]、D[8:1]、
orD[17:0]

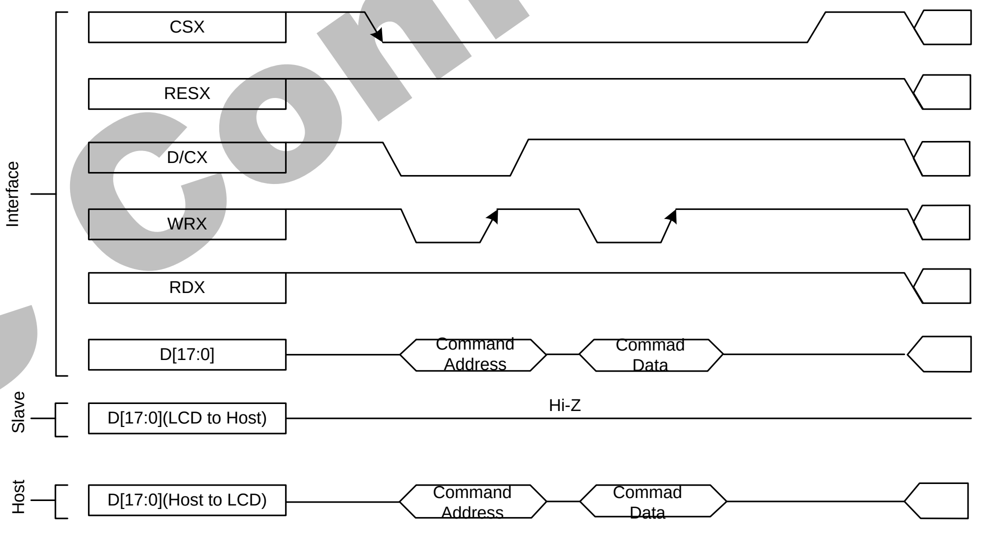
The host asserts D[17:0] 、D[17:10]、D[8:1]、D[17:9] or D[17:10] lines when there is falling edge of WRX

The display read D[17:0] 、D[17:10]、D[8:1]、D[17:9] or D[17:10] lines when there is rising edge of WRX

The host negates D[17:0] 、D[17:10]、D[8:1]、D[17:9] or D[17:10] lines

Note: WRX is an unsynchronized signal (It can be stopped)

Figure 7.


CSX
RESX
D/CX
WRX
RDX
D[17:0]
Command Address
Commad Data
Interface
Slave
D[17:0](LCD to Host)
Hi-Z
Host
D[17:0](Host to LCD)
Command Address
Commad Data

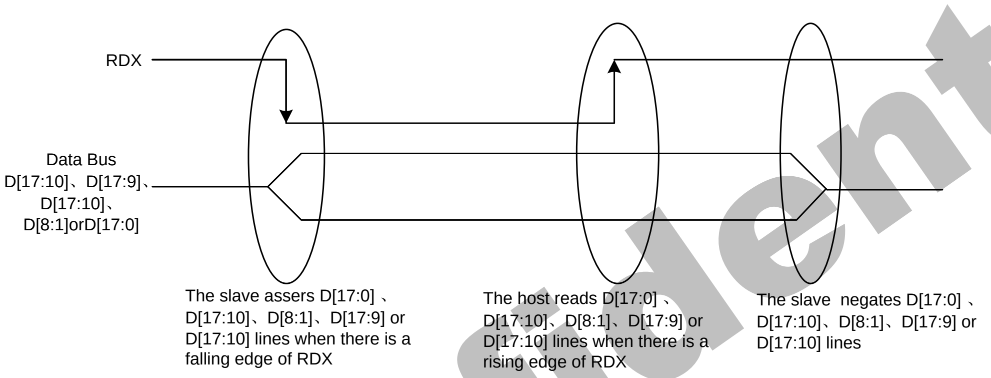
Signals on D[17:0],D/CX,RDX and WRX wires during CSX=" H" are ignored

2.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

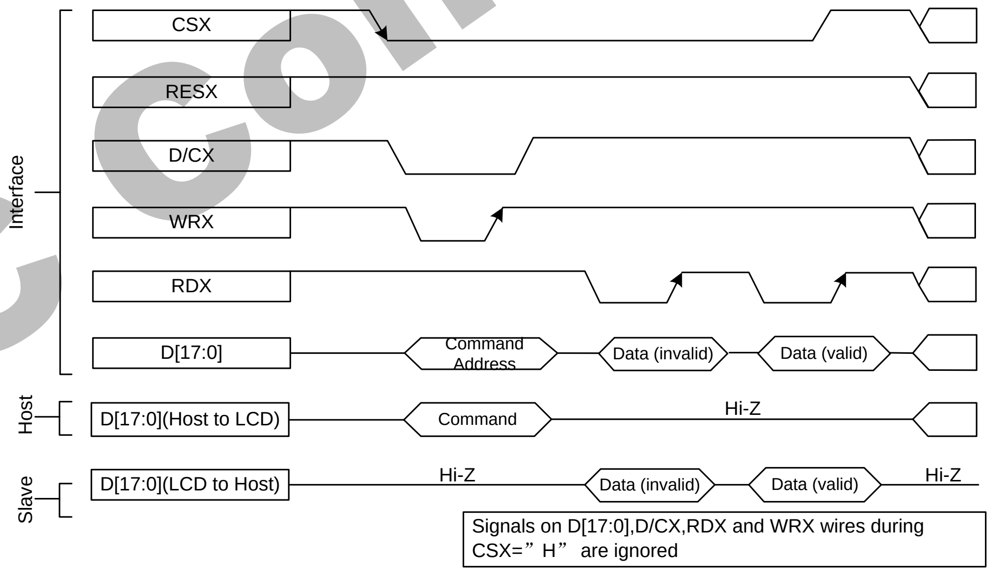
The following figure shows the read cycle for the 8080-II MCU interface.

Figure 8.


RDX
Data Bus
D[17:10]、D[17:9]、
D[17:10]、
D[8:1]orD[17:0]
The slave assers D[17:0] 、D[17:10]、D[8:1]、D[17:9] or D[17:10] lines when there is a falling edge of RDX
The host reads D[17:0] 、D[17:10]、D[8:1]、D[17:9] or D[17:10] lines when there is a rising edge of RDX
The slave negates D[17:0] 、D[17:10]、D[8:1]、D[17:9] or D[17:10] lines

Note: RDX is an unsynchronized signal (It can be stopped).

Figure 9.


CSX
RESX
D/CX
WRX
RDX
D[17:0]
Command Address
Data (invalid)
Data (valid)
Interface
Host
D[17:0](Host to LCD)
Command
Hi-Z
Slave
D[17:0](LCD to Host)
Hi-Z
Data (invalid)
Data (valid)
Hi-Z
Signals on D[17:0],D/CX,RDX and WRX wires during CSX=” H” are ignored

Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

2.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

Table 8.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	1	0	1	3-line serial interface I	“L”	-	↑	Read/Write command, parameter or display data.
1	1	1	1	4-line serial interface I	“L”	"H/L"	↑	Read/Write command, parameter or display data.
1	0	0	1	3-line serial interface II	“L”	-	↑	Read/Write command, parameter or display data.
1	0	1	1	4-line serial interface II	“L”	"H/L"	↑	Read/Write command, parameter or display data.

GC9D01N supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9D01N. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

2.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to GC9D01N. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9D01N and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Figure 10.

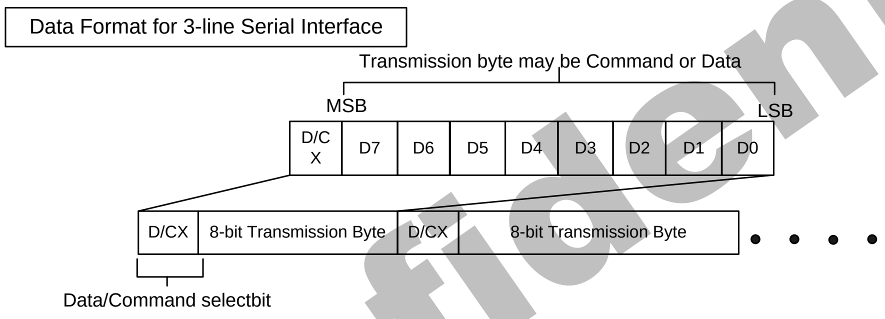
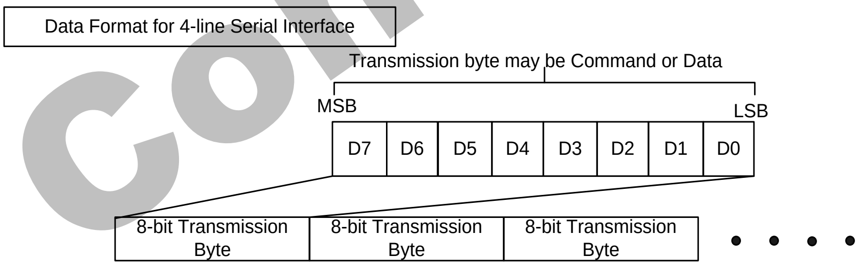
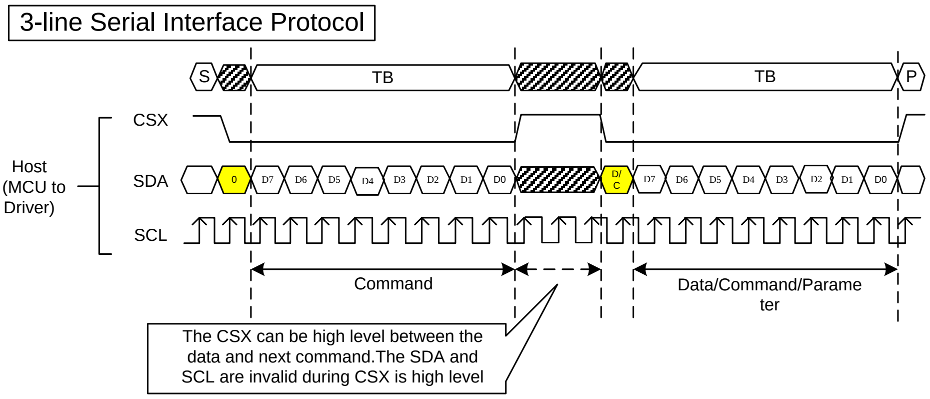

Data Format for 3-line Serial Interface
Transmission byte may be Command or Data
MSB
LSB
D/CX
D7
D6
D5
D4
D3
D2
D1
D0
D/CX
8-bit Transmission Byte
D/CX
8-bit Transmission Byte
Data/Command selectbit

Figure11.


Data Format for 4-line Serial Interface
Transmission byte may be Command or Data
MSB
LSB
D7
D6
D5
D4
D3
D2
D1
D0
8-bit Transmission Byte
8-bit Transmission Byte
8-bit Transmission Byte

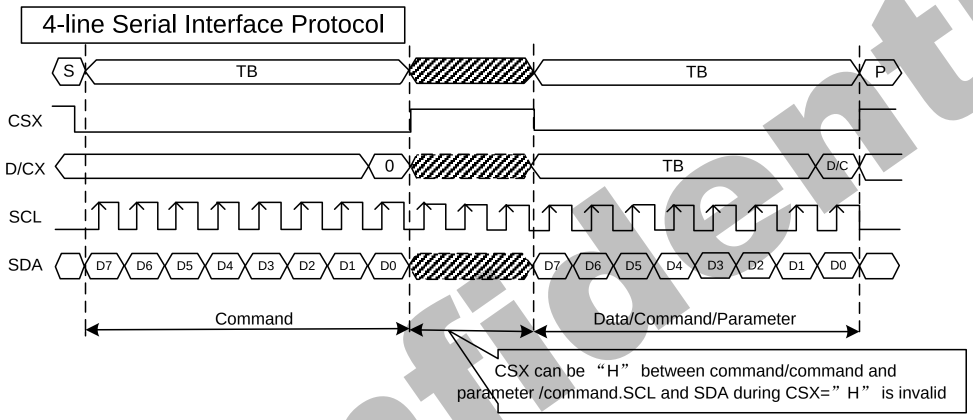
Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9D01N on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

Figure 12.


3-line Serial Interface Protocol
S
TB
TB
P
Host (MCU to Driver)
CSX
SDA
SCL
0
D7
D6
D5
D4
D3
D2
D1
D0
D/C
Command
Data/Command/Parameter

The CSX can be high level between the data and next command.The SDA and SCL are invalid during CSX is high level

Figure 13.


4-line Serial Interface Protocol
S
TB
TB
P
CSX
D/CX
SCL
SDA
0
D/C
D7
D6
D5
D4
D3
D2
D1
D0
Command
Data/Command/Parameter

CSX can be “H” between command/command and parameter /command.SCL and SDA during CSX=”H” is invalid

2.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register’s parameter from GC9D01N. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9D01N latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

Figure 14.

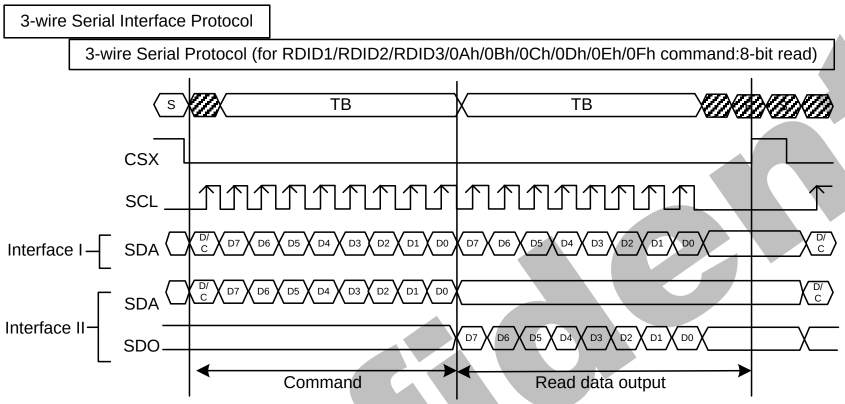

3-wire Serial Interface Protocol
3-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)
S
TB
TB
CSX
SCL
Interface I
SDA
D/C
D7
D6
D5
D4
D3
D2
D1
D0
Interface II
SDA
SDO
Command
Read data output

Figure 15.

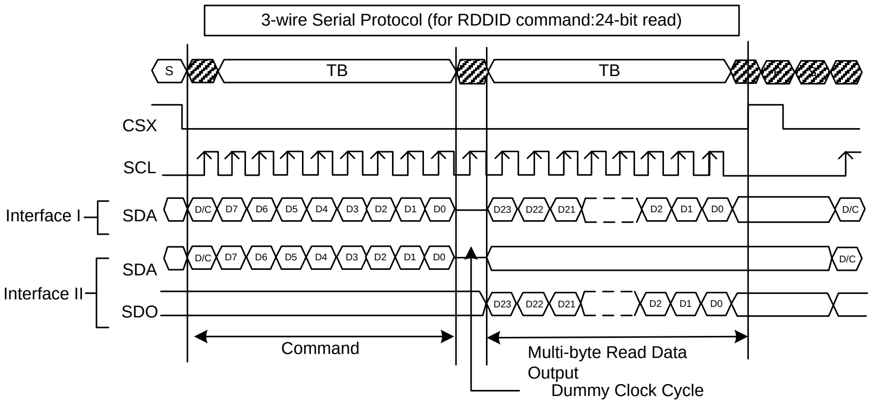

3-wire Serial Protocol (for RDDID command:24-bit read)
S
TB
TB
CSX
SCL
Interface I
SDA
D/C
D7
D6
D5
D4
D3
D2
D1
D0
D23
D22
D21
D2
D1
D0
D/C
Interface II
SDA
SDO
Command
Multi-byte Read Data
Output
Dummy Clock Cycle

Figure 16.

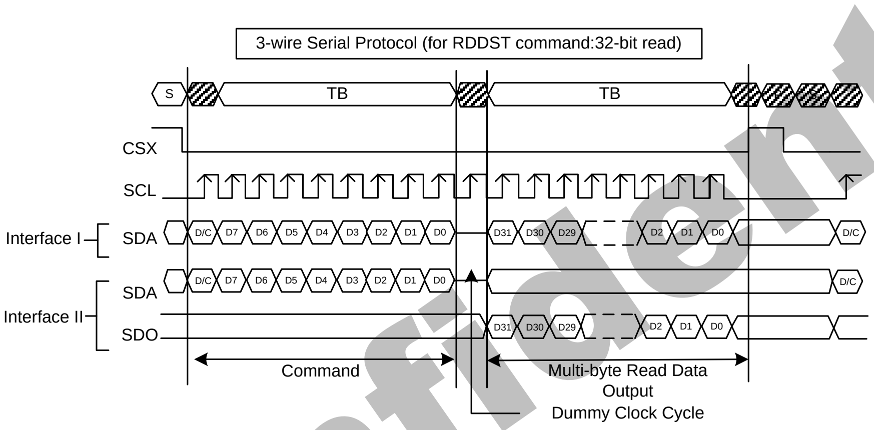

3-wire Serial Protocol (for RDDST command:32-bit read)
S
TB
TB
CSX
SCL
Interface I
SDA
D/C
D7
D6
D5
D4
D3
D2
D1
D0
D31
D30
D29
D2
D1
D0
D/C
Interface II
SDA
SDO
Command
Multi-byte Read Data
Output
Dummy Clock Cycle

Figure 17.

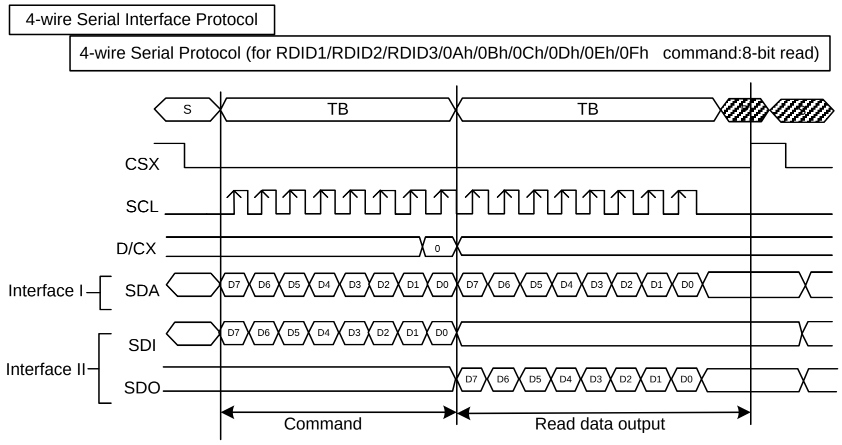

4-wire Serial Interface Protocol
4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)
S
TB
TB
CSX
SCL
D/CX
0
Interface I
SDA
D7 D6 D5 D4 D3 D2 D1 D0
D7 D6 D5 D4 D3 D2 D1 D0
Interface II
SDI
D7 D6 D5 D4 D3 D2 D1 D0
SDO
D7 D6 D5 D4 D3 D2 D1 D0
Command
Read data output

Figure 18.

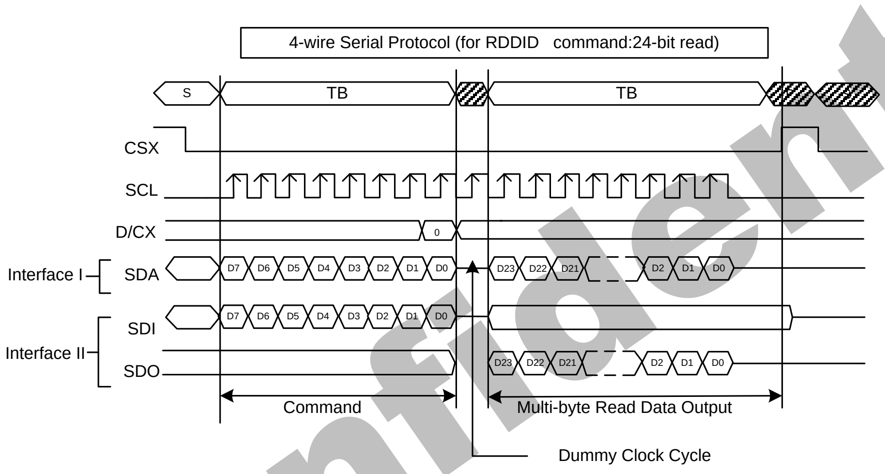
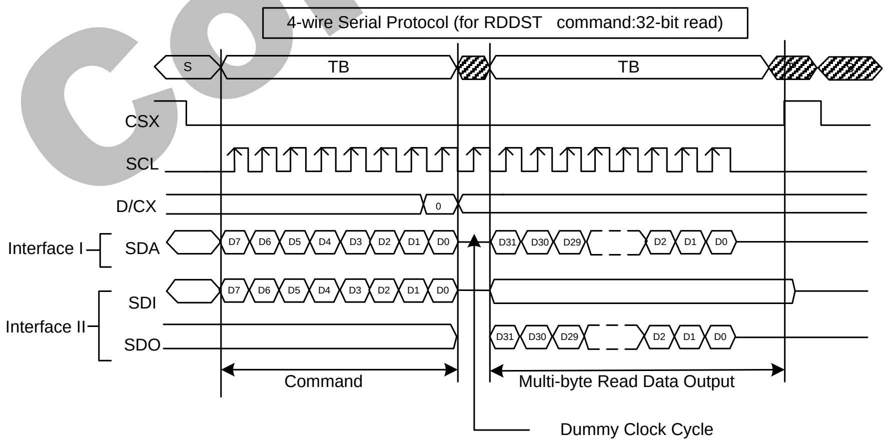

4-wire Serial Protocol (for RDDID command:24-bit read)
S
TB
TB
CSX
SCL
D/CX
0
Interface I
SDA
D7 D6 D5 D4 D3 D2 D1 D0
D23 D22 D21 D2 D1 D0
Interface II
SDI
D7 D6 D5 D4 D3 D2 D1 D0
SDO
D23 D22 D21 D2 D1 D0
Command
Multi-byte Read Data Output
Dummy Clock Cycle

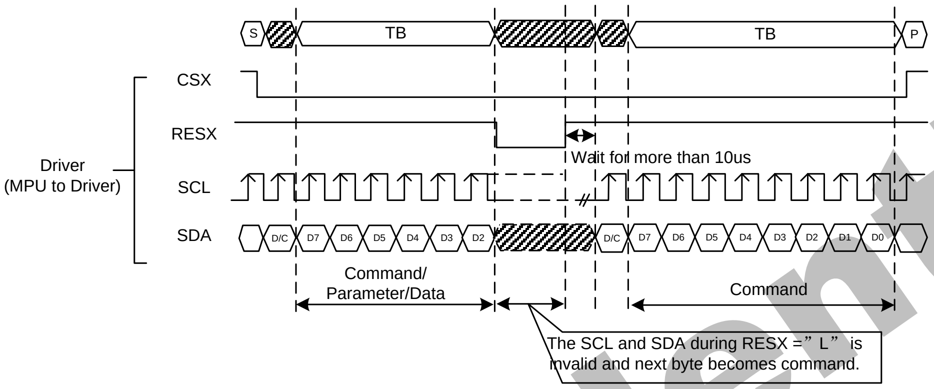
Figure 19.


4-wire Serial Protocol (for RDDST command:32-bit read)
S
TB
TB
CSX
SCL
D/CX
0
Interface I
SDA
D7 D6 D5 D4 D3 D2 D1 D0
D31 D30 D29 D2 D1 D0
Interface II
SDI
D7 D6 D5 D4 D3 D2 D1 D0
SDO
D31 D30 D29 D2 D1 D0
Command
Multi-byte Read Data Output
Dummy Clock Cycle

2.1.11. Data Transfer Break and Recovery

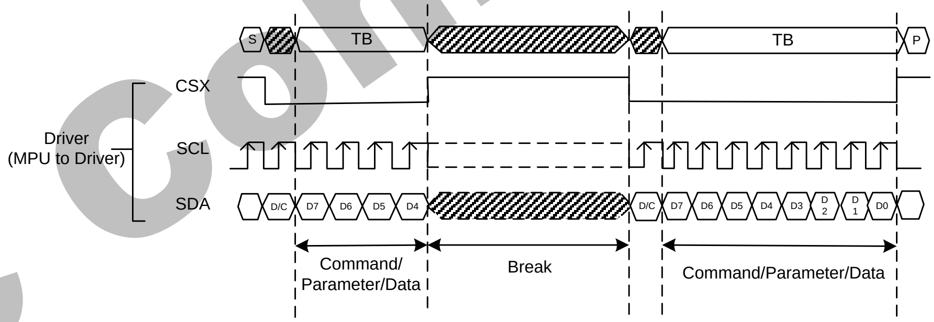
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

Figure 20.


S
TB
TB
P
CSX
RESX
Driver
(MPU to Driver)
SCL
SDA
Wait for more than 10us
D/C
D7
D6
D5
D4
D3
D2
D/C
D7
D6
D5
D4
D3
D2
D1
D0
Command/
Parameter/Data
Command
The SCL and SDA during RESX =" L" is invalid and next byte becomes command.

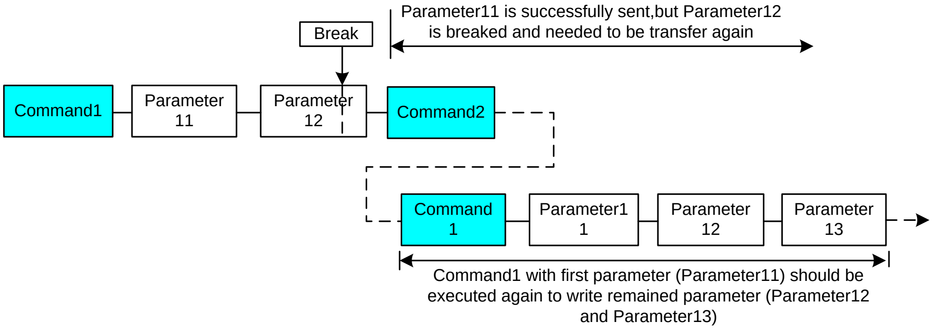
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

Figure 21.


S
TB
TB
P
CSX
Driver
(MPU to Driver)
SCL
SDA
D/C
D7
D6
D5
D4
D/C
D7
D6
D5
D4
D3
D2
D1
D0
Command/
Parameter/Data
Break
Command/Parameter/Data

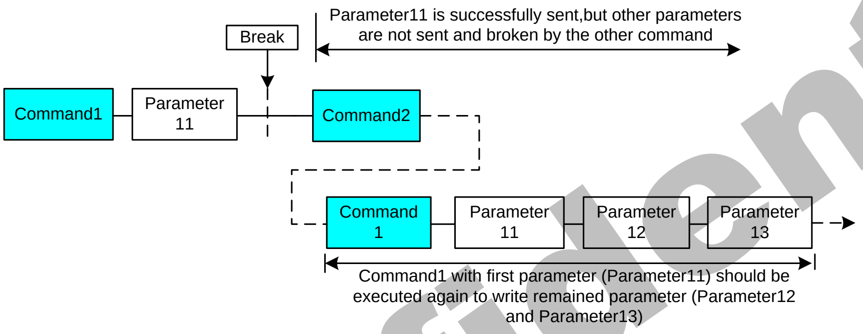
If two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

Figure 22.


Break
Parameter11 is successfully sent,but Parameter12 is breaked and needed to be transfer again
Command1
Parameter 11
Parameter 12
Command2
Command 1
Parameter1 1
Parameter 12
Parameter 13
Command1 with first parameter (Parameter11) should be executed again to write remained parameter (Parameter12 and Parameter13)

If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

Figure 23.

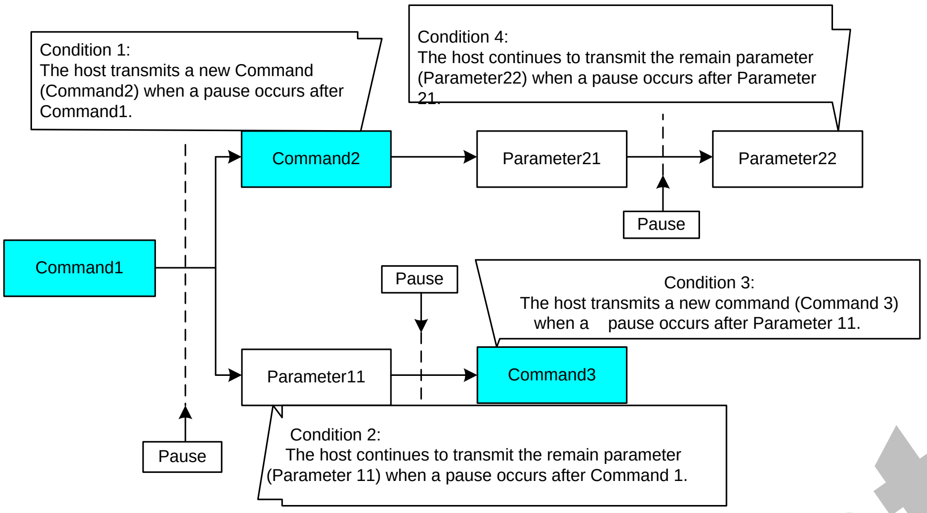

Break
Parameter11 is successfully sent,but other parameters are not sent and broken by the other command
Command1
Parameter 11
Command2
Command 1
Parameter 11
Parameter 12
Parameter 13
Command1 with first parameter (Parameter11) should be executed again to write remained parameter (Parameter12 and Parameter13)

2.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9D01N will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command’s parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

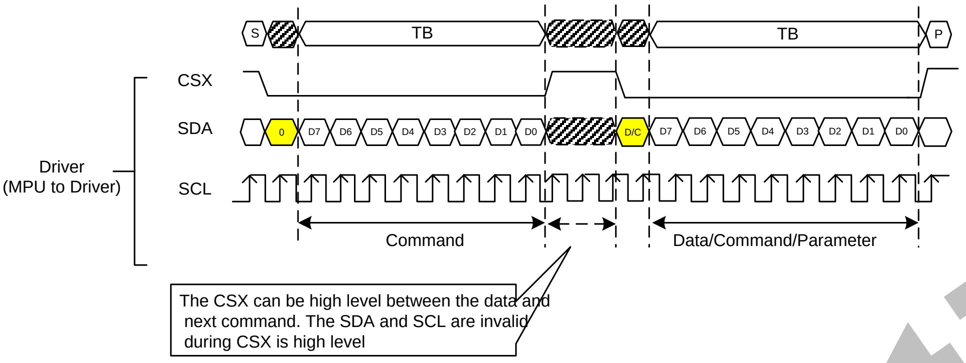
This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Figure 24.


Condition 1:
The host transmits a new Command (Command2) when a pause occurs after Command1.
Condition 4:
The host continues to transmit the remain parameter (Parameter22) when a pause occurs after Parameter 21.
Command2
Parameter21
Parameter22
Pause
Command1
Pause
Condition 3:
The host transmits a new command (Command 3) when a pause occurs after Parameter 11.
Parameter11
Command3
Pause
Condition 2:
The host continues to transmit the remain parameter (Parameter 11) when a pause occurs after Command 1.

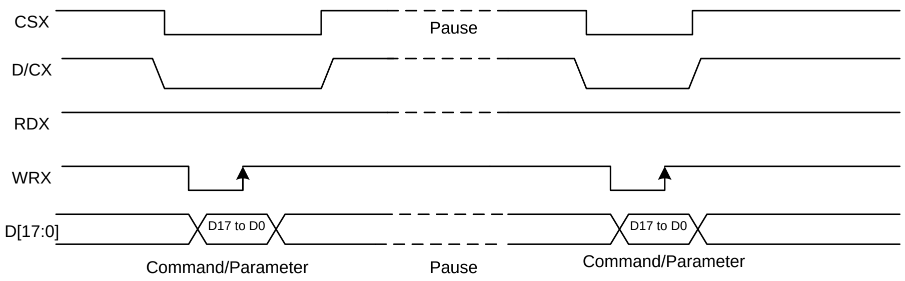
2.1.13. Serial Interface Pause (3_wire)

Figure 25.


S
TB
TB
P
CSX
SDA
SCL
Driver
(MPU to Driver)
0
D7
D6
D5
D4
D3
D2
D1
D0
D/C
D7
D6
D5
D4
D3
D2
D1
D0
Command
Data/Command/Parameter
The CSX can be high level between the data and next command. The SDA and SCL are invalid during CSX is high level

2.1.14. Parallel Interface Pause

Figure 26.


CSX
D/CX
RDX
WRX
D[17:0]
Pause
D17 to D0
D17 to D0
Command/Parameter
Pause
Command/Parameter

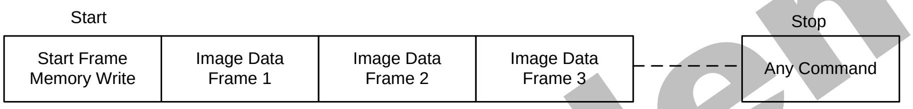
2.1.15. Data Transfer Mode

GC9D01N can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

2.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.

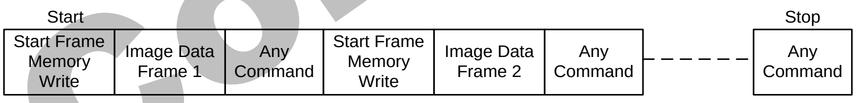
Figure 27.


Start
Start Frame Memory Write
Image Data Frame 1
Image Data Frame 2
Image Data Frame 3
Stop
Any Command

2.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.

Figure 28.


Start
Start Frame Memory Write
Image Data Frame 1
Any Command
Start Frame Memory Write
Image Data Frame 2
Any Command
Stop
Any Command

Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

2.2. RGB Interface

2.2.1. RGB Interface Selection

GC9D01N has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC,DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

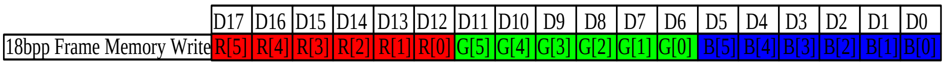
GC9D01N supports several pixel formats that can be selected by RIM bit of F6h command. The selection of a given interfaces is done by setting RCM [1:0] as show in the following table.

Table 9

RCM[1:0]		RIM	DPI[1:0]			RGB interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC,HSYNC,DE,DOTCLK,D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DE,DOTCLK,D[17:13] & D[11:1]
1	0	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DE,DOTCLK,D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command	VSYNC,HSYNC,DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]
1	1	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , RIM=0

Figure 29.



	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

Figure 30.

	D17	D16	D15	D14	D13	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color are same as MSB data.

6-bit data bus interface (D[5:0] is used) , RIM=1

Figure 31.

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D[17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal. In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of DOTCLK). D [17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.

Figure32.

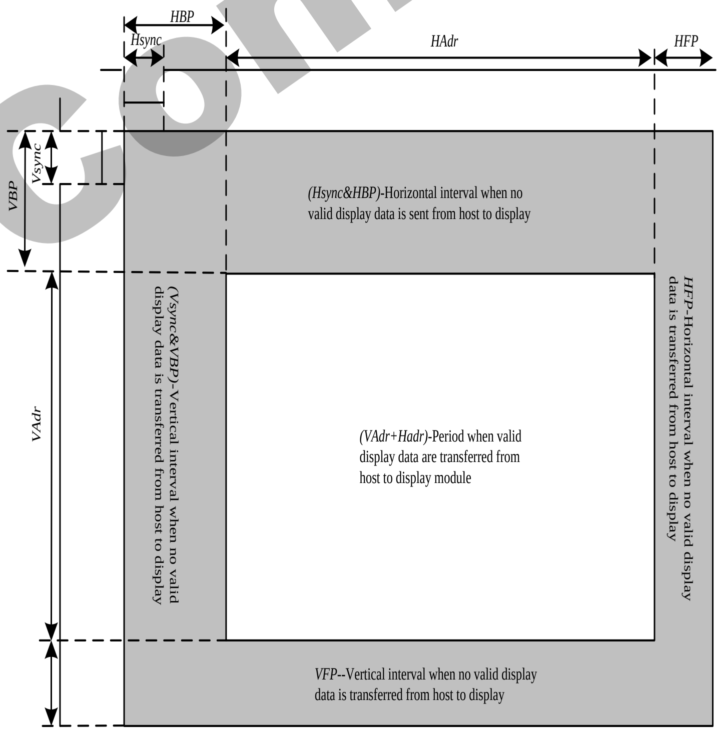

HBP
Hsync
HAdr
HFP
VBP
Vsync
VAdr
(Hsync&HBP)-Horizontal interval when no valid display data is sent from host to display
(Vsync&VBP)-Vertical interval when no valid display data is transferred from host to display
HFP-Horizontal interval when no valid display data is transferred from host to display
(VAdr+Hadr)-Period when valid display data are transferred from host to display module
VFP--Vertical interval when no valid display data is transferred from host to display

Table 10.

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	160	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	160	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Notes:

1. Vertical period (one frame) shall be equal to the sum of VBP + VAdr + VFP.

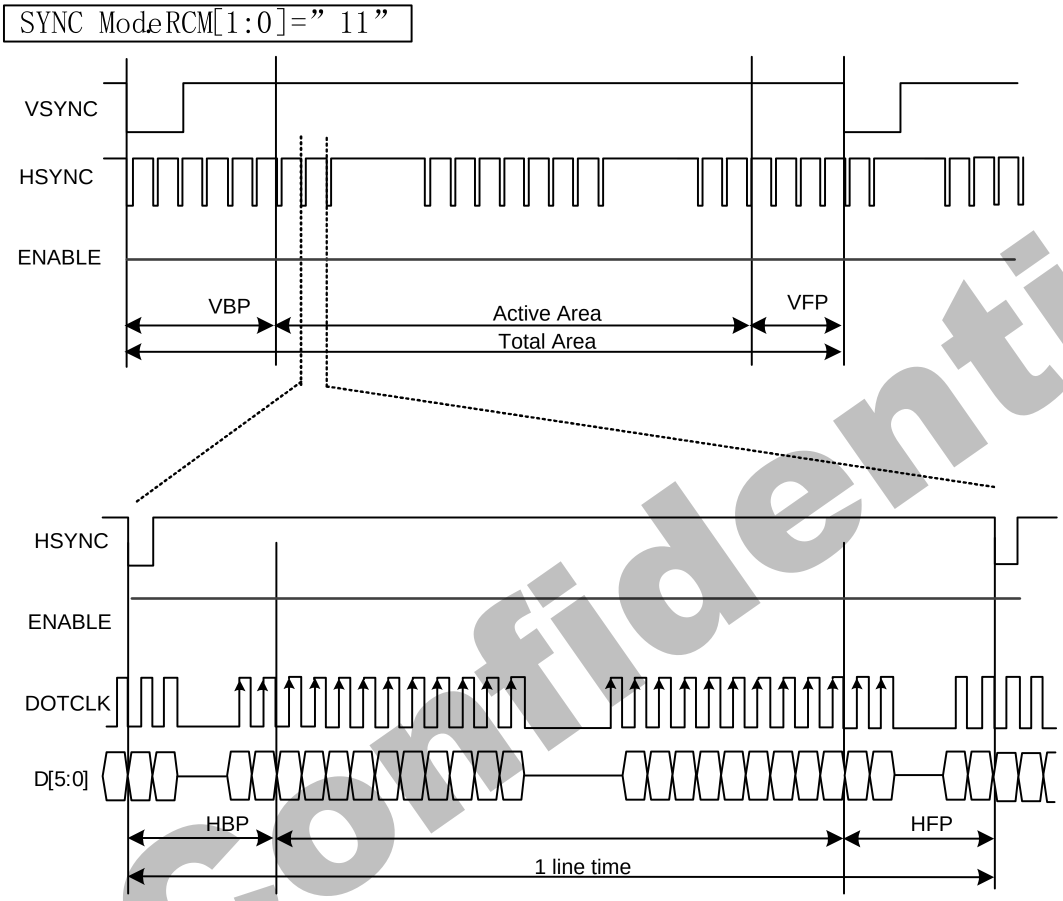
2. Horizontal period (one line) shall be equal to the sum of HBP + HAdr + HFP.

3. Control signals Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

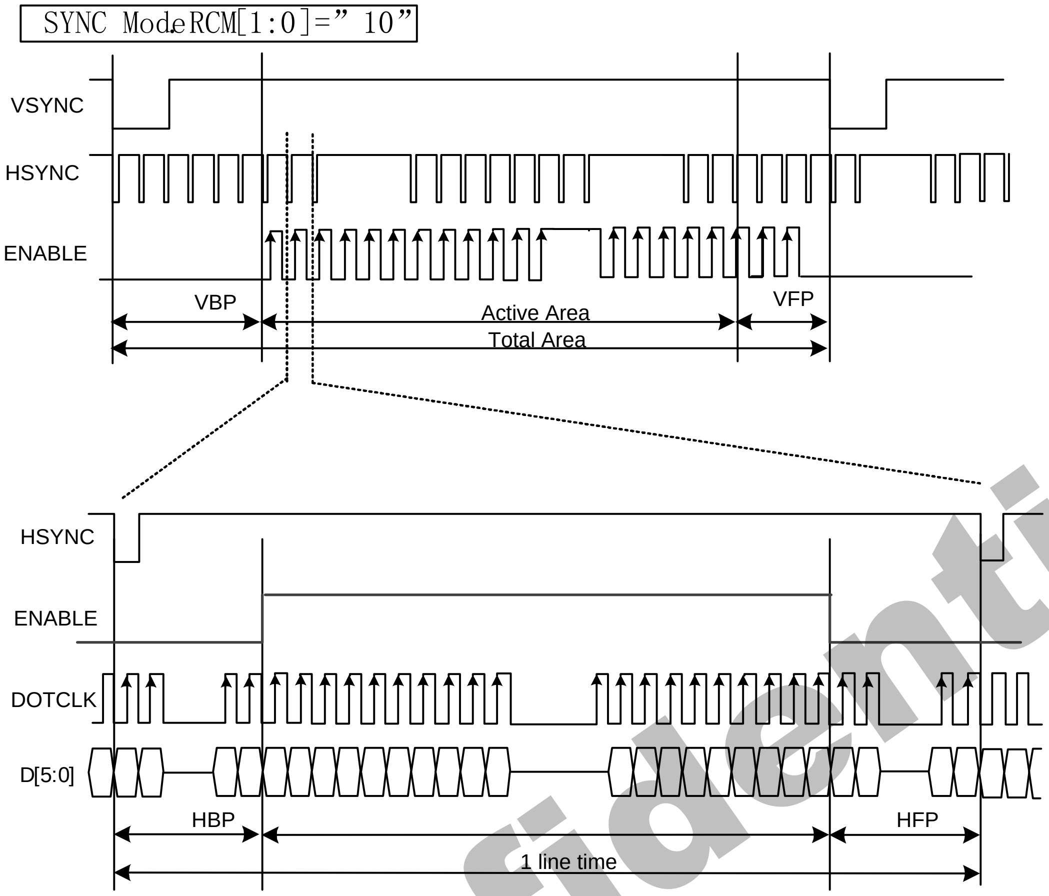
2.2.2. RGB Interface Timing

The timing chart of 18/16-bit RGB interface mode1 and mode 2 is shown as below.

Figure33.


SYNC ModeRCM[1:0]=" 11"
VSYNC
HSYNC
ENABLE
VBP
Active Area
VFP
Total Area
HSYNC
ENABLE
DOTCLK
D[5:0]
HBP
HFP
1 line time

Mode1 RGB SYNC mode


SYNC Mode RCM[1:0]=" 10"
VSYNC
HSYNC
ENABLE
VBP
Active Area
VFP
Total Area
HSYNC
ENABLE
DOTCLK
D[5:0]
HBP
HFP
1 line time

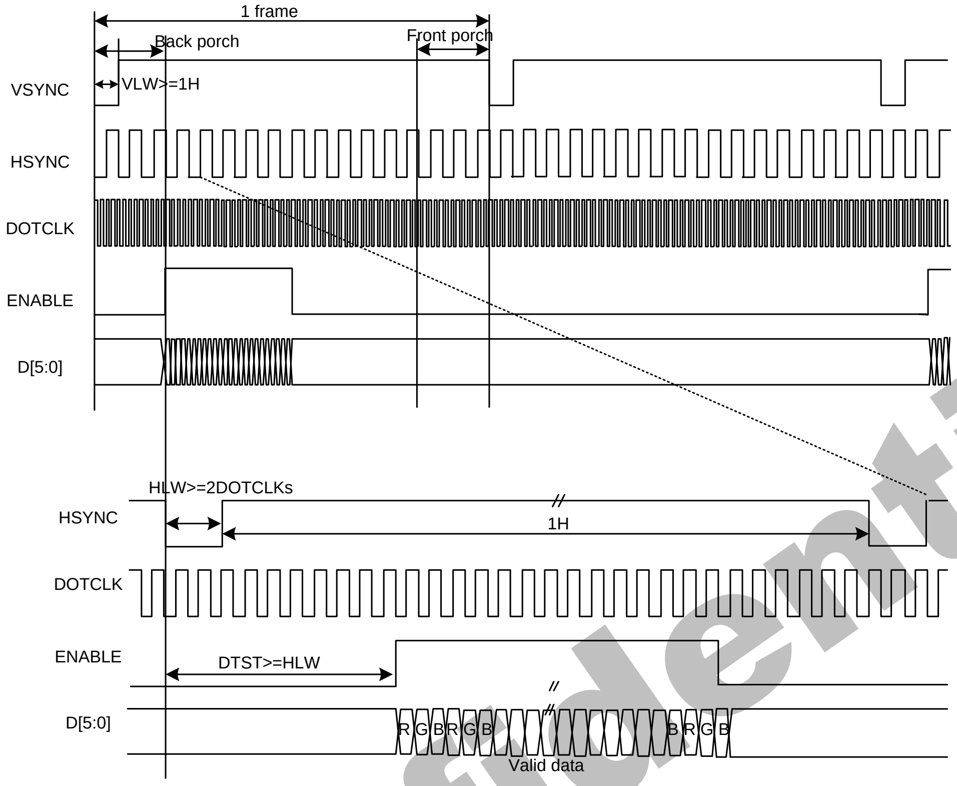
Mode2 RGB SYNC+DE mode

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:

Figure34.


1 frame
Back porch
Front porch
VLW>=1H
VSYNC
HSYNC
DOTCLK
ENABLE
D[5:0]
HLW>=2DOTCLKs
1H
DTST>=HLW
R G B R G B
B R G B
Valid data

VLW: VSYNC Low Width
HLW: HSYNC Low Width
DTST: Data Transfer Startup Time

Note 1: 6-bit RGB interface mode only used in the DE interface.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

2.3. Display Data RAM (DDRAM)

GC9D01N has an integrated 360x360x18-bit graphic type static RAM. This 291,600 -bytes memory allows storing a 36xRGBx360 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

2.4. Display Data Format

GC9D01N supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

2.4.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9D01N can be used by setting external pin as IM [3:0] to “1101” for serial interface I, IM [3:0] to “1001” for serial interface II. The shown figure is the example of 3-line SPI interface.

Figure39.

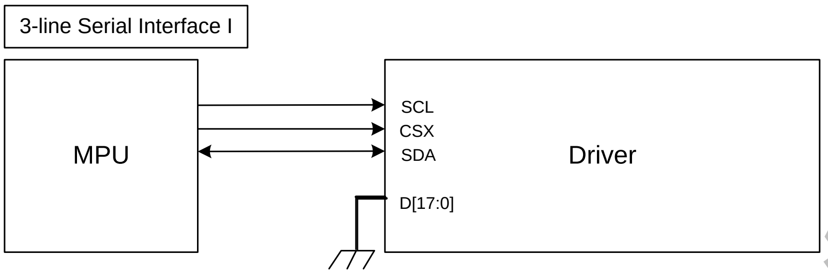
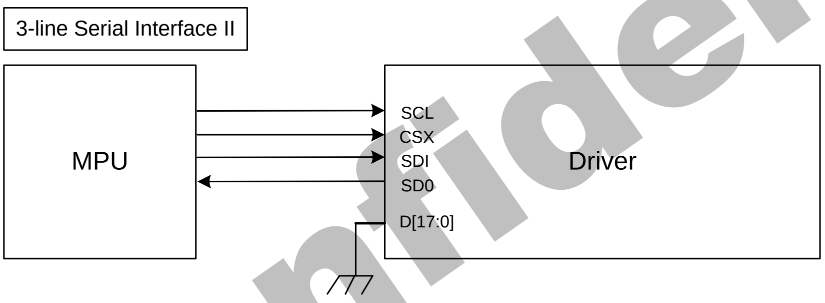

3-line Serial Interface I
MPU
SCL
CSX
SDA
D[17:0]
Driver

Figure40.


3-line Serial Interface II
MPU
SCL
CSX
SDI
SD0
D[17:0]
Driver

In 3-line serial interface, different display data format is available for three color depths supported by the LCM listed below.

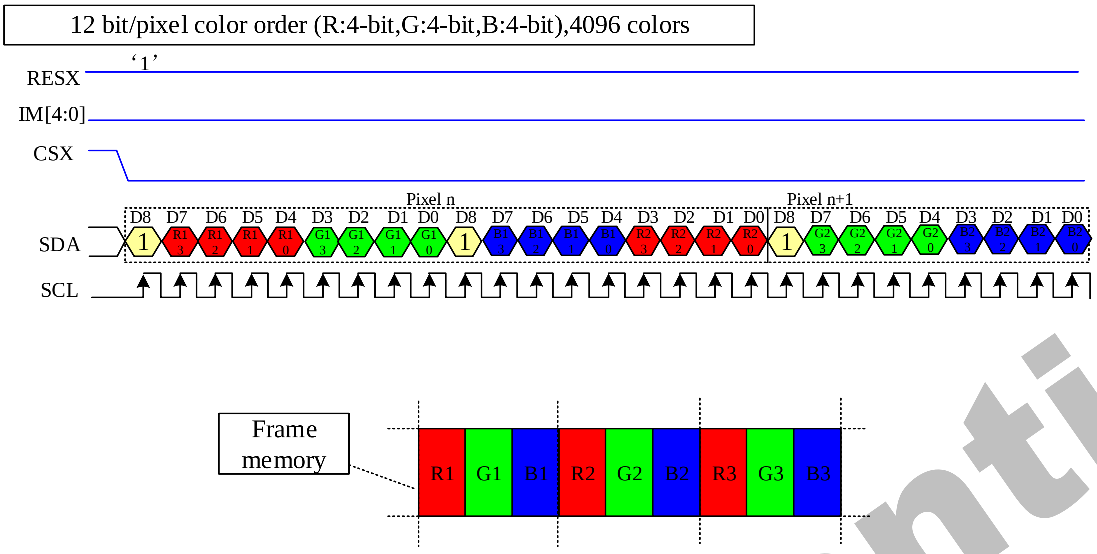
-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

1)4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Figure41.


12 bit/pixel color order (R:4-bit,G:4-bit,B:4-bit),4096 colors
‘1’
RESX
IM[4:0]
CSX
SDA
SCL
Pixel n
Pixel n+1
D8 D7 D6 D5 D4 D3 D2 D1 D0 D8 D7 D6 D5 D4 D3 D2 D1 D0 D8 D7 D6 D5 D4 D3 D2 D1 D0
1 R13 R12 R11 R10 G13 G12 G11 G10 1 B13 B12 B11 B10 R23 R22 R21 R20 1 G23 G22 G21 G20 B23 B22 B21 B20
Frame memory
R1 G1 B1 R2 G2 B2 R3 G3 B3

Note 1: The pixel data with 12-bit color depth information.

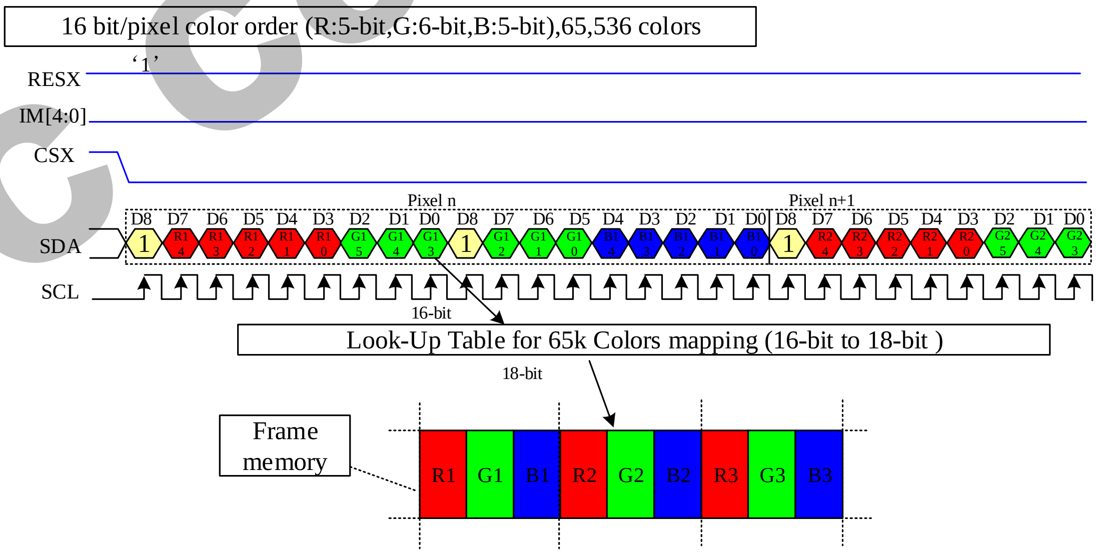
Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: ‘-‘= Don’t care –Can be set “0” or “1”.

2)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

Figure41.


16 bit/pixel color order (R:5-bit,G:6-bit,B:5-bit),65,536 colors
‘1’
RESX
IM[4:0]
CSX
SDA
SCL
Pixel n
Pixel n+1
D8 D7 D6 D5 D4 D3 D2 D1 D0 D8 D7 D6 D5 D4 D3 D2 D1 D0 D8 D7 D6 D5 D4 D3 D2 D1 D0
1 R14 R13 R12 R11 R10 G15 G14 G13 1 G12 G11 G10 B14 B13 B12 B11 B10 1 R24 R23 R22 R21 R20 G25 G24 G23
16-bit
Look-Up Table for 65k Colors mapping (16-bit to 18-bit)
18-bit
Frame memory
R1 G1 B1 R2 G2 B2 R3 G3 B3

Note 1: The pixel data with 16-bit color depth information.

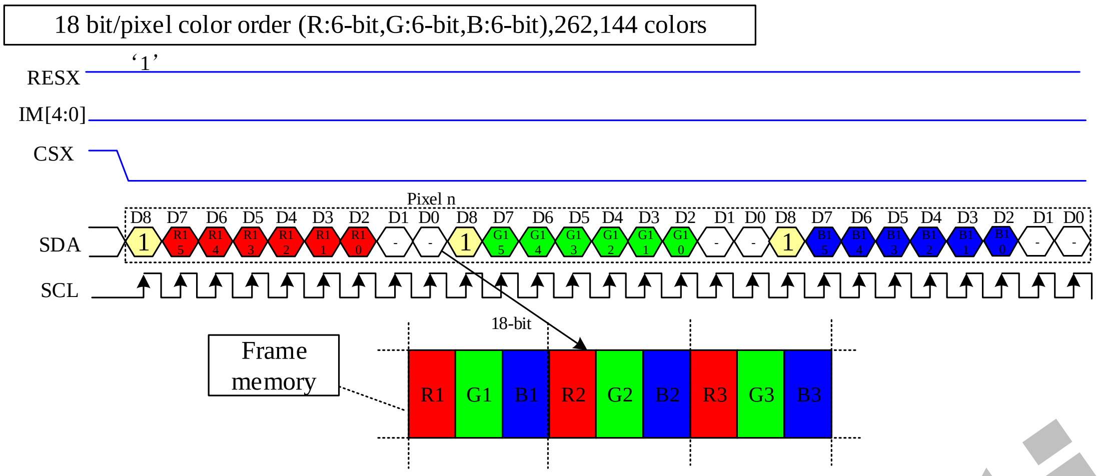
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: ‘-‘= Don’t care –Can be set “0” or “1”.

3)262K-Colors:18-bit/pixel (RGB 6, 6, 6 -bits input).

Figure42.


18 bit/pixel color order (R:6-bit,G:6-bit,B:6-bit),262,144 colors
'1'
RESX
IM[4:0]
CSX
Pixel n
SDA
D8 D7 D6 D5 D4 D3 D2 D1 D0 D8 D7 D6 D5 D4 D3 D2 D1 D0 D8 D7 D6 D5 D4 D3 D2 D1 D0
1 R15 R14 R13 R12 R11 R10 - - 1 G15 G14 G13 G12 G11 G10 - - 1 B15 B14 B13 B12 B11 B10 - -
SCL
18-bit
Frame memory
R1 G1 B1 R2 G2 B2 R3 G3 B3

Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

2.4.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9D01N can be used by setting external pin as IM [3:0] to “1111” for serial interface I , IM [3:0] to “1011” for serial interfaceII . The shown figure is the example of 4-line SPI interface.

Figure43.

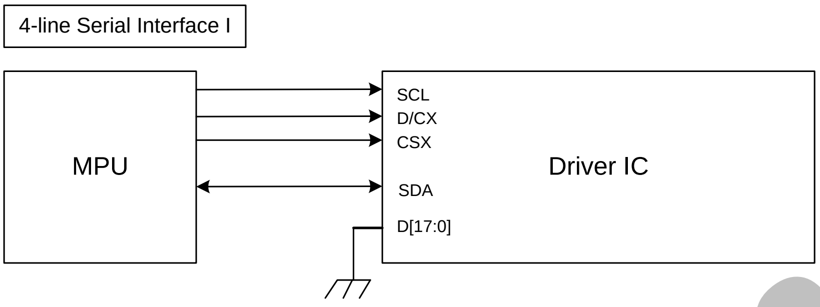
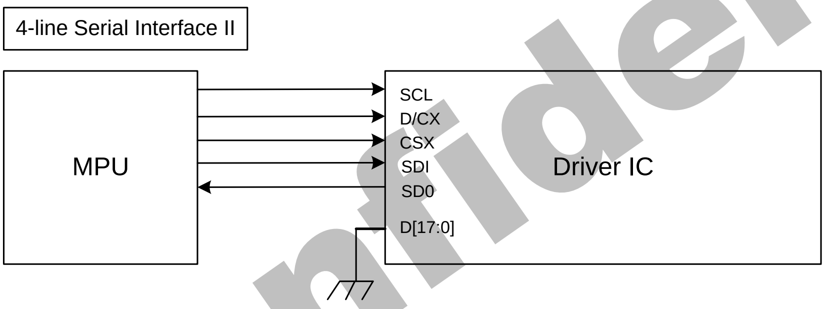

4-line Serial Interface I
MPU
SCL
D/CX
CSX
SDA
D[17:0]
Driver IC

Figure44.


4-line Serial Interface II
MPU
SCL
D/CX
CSX
SDI
SD0
D[17:0]
Driver IC

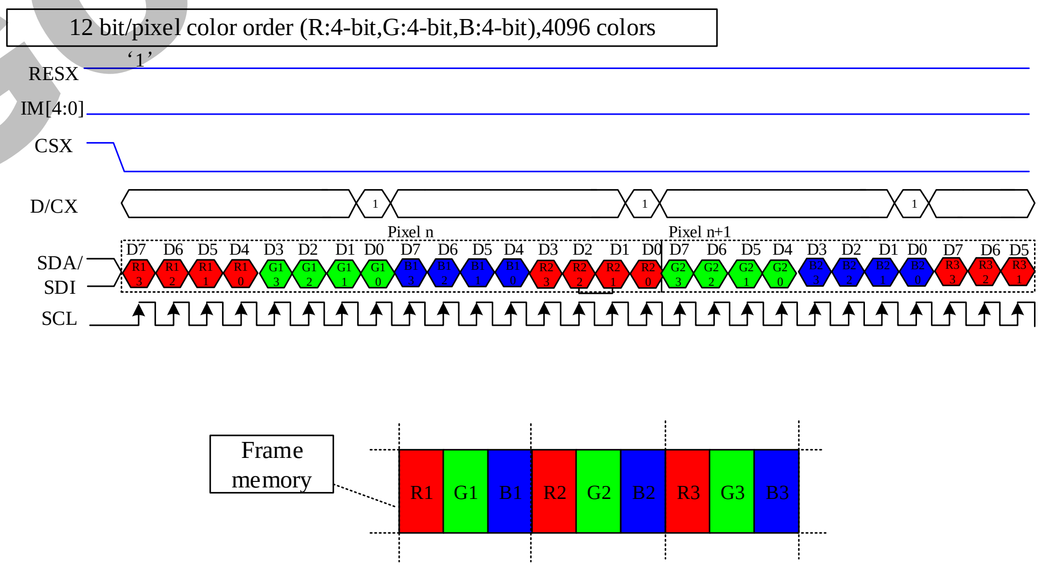
In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

Figure44.


12 bit/pixel color order (R:4-bit,G:4-bit,B:4-bit),4096 colors
‘1’
RESX
IM[4:0]
CSX
D/CX
1
1
1
Pixel n
Pixel n+1
SDA/
SDI
SCL
D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5
Frame memory
R1 G1 B1 R2 G2 B2 R3 G3 B3

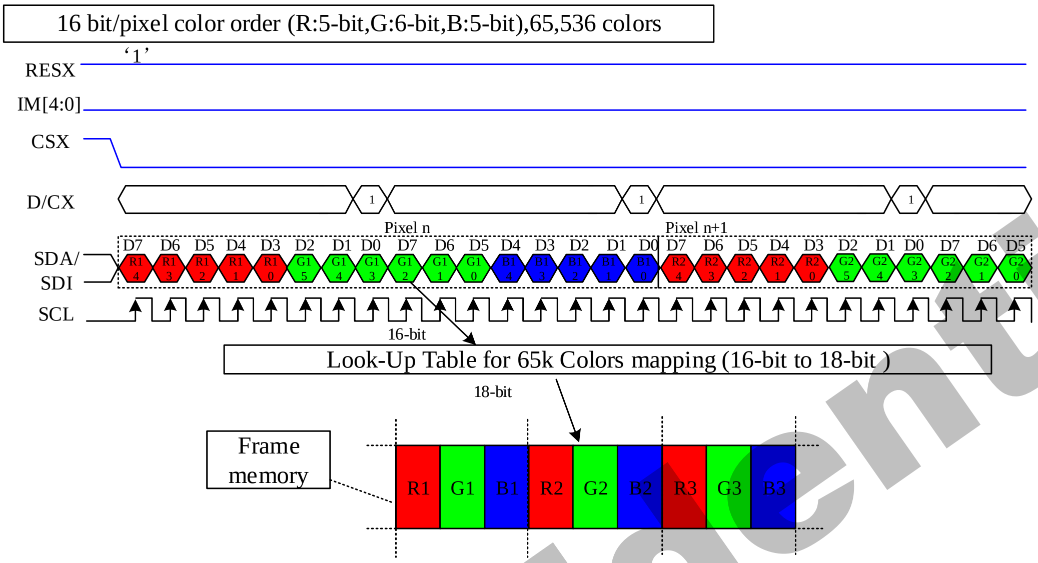
Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure45.


16 bit/pixel color order (R:5-bit,G:6-bit,B:5-bit),65,536 colors
'1'
RESX
IM[4:0]
CSX
D/CX
1
1
1
Pixel n
Pixel n+1
SDA/
SDI
D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5
SCL
16-bit
Look-Up Table for 65k Colors mapping (16-bit to 18-bit)
18-bit
Frame
memory
R1 G1 B1 R2 G2 B2 R3 G3 B3

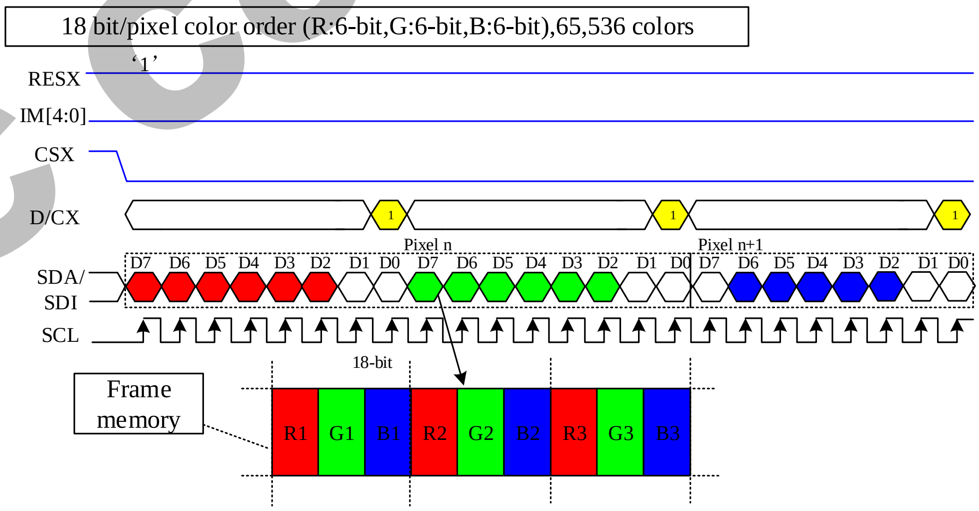
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure46.


18 bit/pixel color order (R:6-bit,G:6-bit,B:6-bit),65,536 colors
'1'
RESX
IM[4:0]
CSX
D/CX
1
1
1
Pixel n
Pixel n+1
SDA/
SDI
D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0
SCL
18-bit
Frame
memory
R1 G1 B1 R2 G2 B2 R3 G3 B3

Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

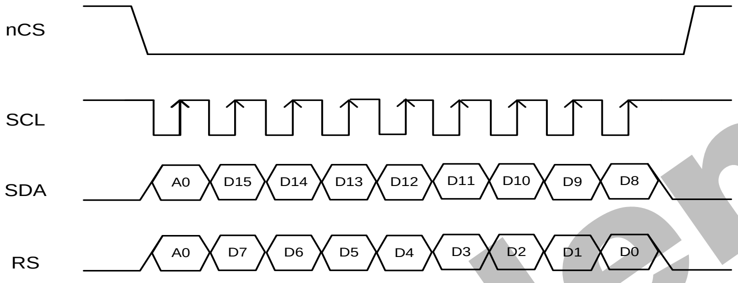
2.4.3. 2-data-lane mode

This mode is active when 2data_en (B1h[3]) set to “1” in 3-wire. Only frame pixel data write transitions are sent in 2-data-lane mode, register write/read is still sent in 3-wire.

The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and DCX (RS)are serial data lines.

Serial data must be input to SDA in the sequence A0, D15 to D10 and DCX(RS) in the sequence A0, D7 to D0. The GC9D01N reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.

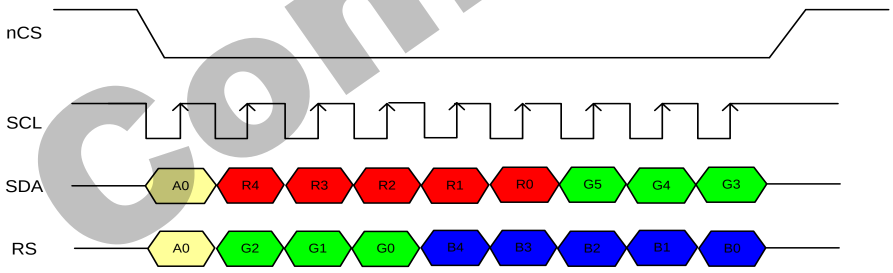
Figure47.


nCS
SCL
SDA
A0
D15
D14
D13
D12
D11
D10
D9
D8
RS
A0
D7
D6
D5
D4
D3
D2
D1
D0

Five data formats are supported in 2-data-lane mode, which is indicated by 2data_mdt (B1h[2:0]) .

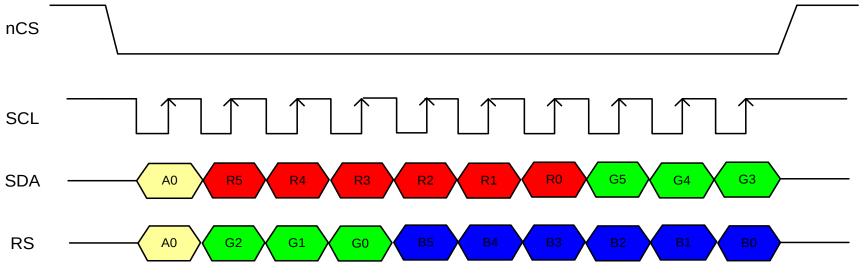
1)RGB565 1pixel/transition(65K color,2data_mdt[2:0]=’000’)

Figure48.


nCS
SCL
SDA
A0
R4
R3
R2
R1
R0
G5
G4
G3
RS
A0
G2
G1
G0
B4
B3
B2
B1
B0

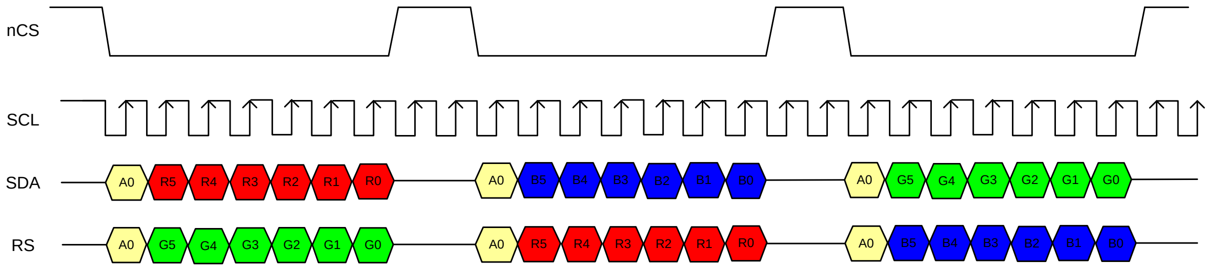
2)RGB666 1pixel/transition(262K color,2data_mdt[2:0]=’001’)

Figure49.


nCS
SCL
SDA
A0
R5
R4
R3
R2
R1
R0
G5
G4
G3
RS
A0
G2
G1
G0
B5
B4
B3
B2
B1
B0

3)RGB666 2/3pixel/transition(262K color,2data_mdt[2:0]='010')

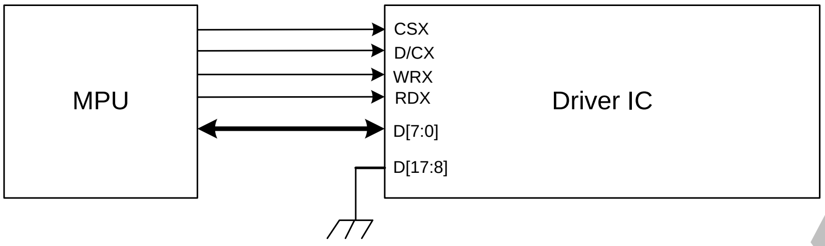
Figure50.


nCS
SCL
SDA
RS
A0
R5
R4
R3
R2
R1
R0
B5
B4
B3
B2
B1
B0
G5
G4
G3
G2
G1
G0

2.4.4. 8-bit Parallel MCU Interface

The 8080- Ⅰ system 8-bit parallel bus interface of GC9D01N can be used by setting external pin as IM [3:0] to“0100”.The following shown figure is the example of interface with 8080- Ⅰ MCU system interface.

Figure53.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table 11.

Count	0	1	2	3	4	…	317	318	319	320
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	158R4	158G2	159R4	159G2
D6	C6	0R3	0G1	1R3	1G1	…	158R3	158G1	159R3	159G1
D5	C5	0R2	0G0	1R2	1G0	…	158R2	158G0	159R2	159G0
D4	C4	0R1	0B4	1R1	1B4	…	158R1	158B4	159R1	159B4
D3	C3	0R0	0B3	1R0	1B3	…	158R0	158B3	159R0	159B3
D2	C2	0G5	0B2	1G5	1B2	…	157G5	158B2	158G5	159B2
D1	C1	0G4	0B1	1G4	1B1	…	157G4	158B1	158G4	159B1
D0	C0	0G3	0B0	1G3	1B0	…	157G3	158B0	158G3	159B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

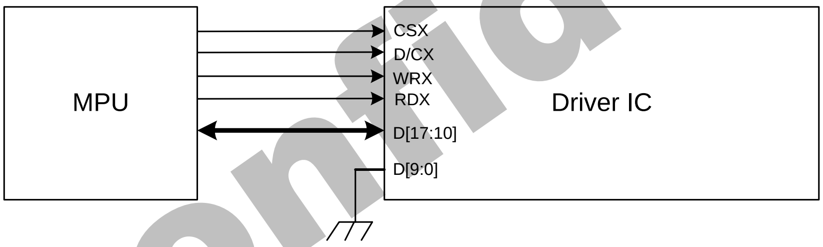
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table12.

Count	0	1	2	3	…	478	479	480
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	159R5	159G5	159B5
D6	C6	0R4	0G4	0B4	…	159R4	159G4	159B4
D5	C5	0R3	0G3	0B3	…	159R3	159G3	159B3
D4	C4	0R2	0G2	0B2	…	159R2	159G2	159B2
D3	C3	0R1	0G1	0B1	…	159R1	159G1	159B1
D2	C2	0R0	0G0	0B0	…	159R0	159G0	159B0
D1	C1				…			
D0	C0				…			

The 8080-II system 8-bit parallel bus interface of GC9D01N can be used by settings as IM [3:0] =”0000”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.

Figure54.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table13.

Count	0	1	2	3	4	…	237	238	239	240
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	158R4	158G2	159R4	159G2
D16	C6	0R3	0G1	1R3	1G1	…	158R3	158G1	159R3	159G1
D15	C5	0R2	0G0	1R2	1G0	…	158R2	158G0	159R2	159G0
D14	C4	0R1	0B4	1R1	1B4	…	158R1	158B4	159R1	159B4
D13	C3	0R0	0B3	1R0	1B3	…	158R0	158B3	159R0	159B3
D12	C2	0G5	0B2	1G5	1B2	…	158G5	158B2	158G5	159B2
D11	C1	0G4	0B1	1G4	1B1	…	158G4	158B1	158G4	159B1
D10	C0	0G3	0B0	1G3	1B0	…	158G3	158B0	158G3	159B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to“110”.

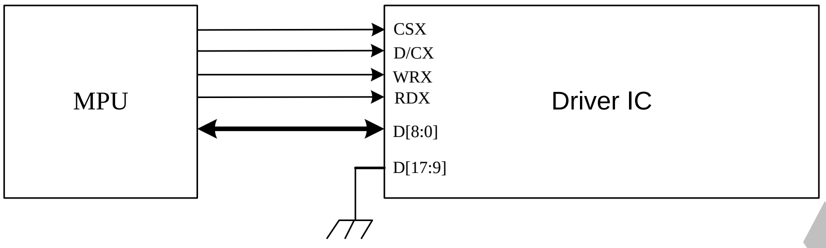
Table14.

Count	0	1	2	3	…	478	479	480
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	159R5	159G5	159B5
D16	C6	0R4	0G4	0B4	…	159R4	159G4	159B4
D15	C5	0R3	0G3	0B3	…	159R3	159G3	159B3
D14	C4	0R2	0G2	0B2	…	159R2	159G2	159B2
D13	C3	0R1	0G1	0B1	…	159R1	159G1	159B1
D12	C2	0R0	0G0	0B0	…	159R0	159G0	159B0
D11	C1				…			
D10	C0				…			

2.4.5. 9-bit Parallel MCU Interface

The 8080-I system 9-bit parallel bus interface of GC9D01N can be selected by setting hardware pin IM [3:0] to “0101”. The following shown figure is the example of interface with 8080- Ⅰ MCU system interface.

Figure55.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

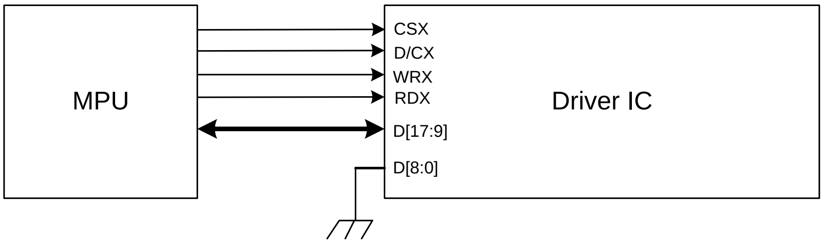
There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

Table15.

Count	0	1	2	3	4	…	317	318	319	320
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2	…	158R5	158G2	159R5	159G2
D7	C7	0R4	0G1	1R4	1G1	…	158R4	158G1	159R4	159G1
D6	C6	0R3	0G0	1R3	1G0	…	358R3	158G0	159R3	159G0
D5	C5	0R2	0B5	1R2	1B5	…	158R2	158B5	159R2	159B5
D4	C4	0R1	0B4	1R1	1B4	…	158R1	158B4	159R1	159B4
D3	C3	0R0	0B3	1R0	1B3	…	158R0	158B3	159R0	159B3
D2	C2	0G5	0B2	1G5	1B2	…	158G5	158B2	159G5	159B2
D1	C1	0G4	0B1	1G4	1B1	…	158G4	158B1	159G4	159B1
D0	C0	0G3	0B0	1G3	1B0	…	158G3	158B0	159G3	159B0

The 8080- Ⅱ system 9-bit parallel bus interface of GC9D01N can be selected by setting hardware pin IM [3:0] to “0001”. The following shown figure is the example of interface with 8080- MCU system interface.

Figure56.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

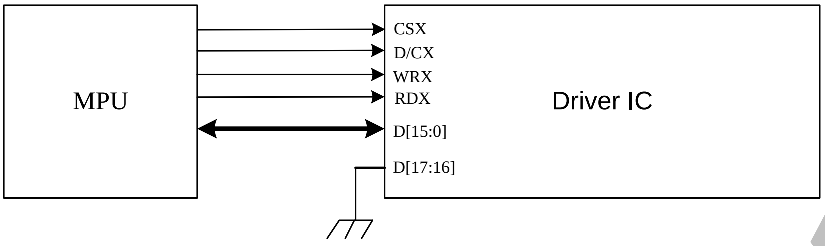
Table16.

Count	0	1	2	3	4	…	317	318	319	320
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	…	158R5	158G2	159R5	159G2
D16	C6	0R4	0G1	1R4	1G1	…	158R4	158G1	159R4	159G1
D15	C5	0R3	0G0	1R3	1G0	…	358R3	158G0	159R3	159G0
D14	C4	0R2	0B5	1R2	1B5	…	158R2	158B5	159R2	159B5
D13	C3	0R1	0B4	1R1	1B4	…	158R1	158B4	159R1	159B4
D12	C2	0R0	0B3	1R0	1B3	…	158R0	158B3	159R0	159B3
D11	C1	0G5	0B2	1G5	1B2	…	158G5	158B2	159G5	159B2
D10	C0	0G4	0B1	1G4	1B1	…	158G4	158B1	159G4	159B1
D9		0G3	0B0	1G3	1B0	…	158G3	158B0	159G3	159B0

2.4.6. 16-bit Parallel MCU Interface

The 8080- Ⅰ system 16-bit parallel bus interface of GC9D01N can be selected by setting hardware pin IM[3:0] to “0110”.The following shown figure is the example of interface with 8080- Ⅰ MCU system interface.

Figure57.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table17.

Count	0	1	2	3	…	158	159	160
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	157R4	158R4	159R4
D14		0R3	1R3	2R3	…	157R3	158R3	159R3
D13		0R2	1R2	2R2	…	157R2	158R2	159R2
D12		0R1	1R1	2R1	…	157R1	158R1	159R1
D11		0R0	1R0	2R0	…	157R0	158R0	159R0
D10		0G5	1G5	2G5	…	157G5	158G5	159G5
D9		0G4	1G4	2G4	…	157G4	158G4	159G4
D8		0G3	1G3	2G3	…	157G3	158G3	159G3
D7	C7	0G2	1G2	2G2	…	157G2	158G2	159G2
D6	C6	0G1	1G1	2G1	…	157G1	158G1	159G1
D5	C5	0G0	1G0	2G0	…	157G0	158G0	159G0
D4	C4	0B4	1B4	2B4	…	157B4	158B4	159B4
D3	C3	0B3	1B3	2B3	…	157B3	158B3	159B3
D2	C2	0B2	1B2	2B2	…	157B2	158B2	159B2
D1	C1	0B1	1B1	2B1	…	157B1	158B1	159B1
D0	C0	0B0	1B0	2B0	…	157B0	158B0	159B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

1)MDT[1:0]=“00”

Table18.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	158R5	158B5	159G5
D14		0R4	0B4	1G4	…	158R4	158B4	159G4
D13		0R3	0B3	1G3	…	158R3	158B3	159G3
D12		0R2	0B2	1G2	…	158R2	158B2	159G2
D11		0R1	0B1	1G1	…	158R1	158B1	159G1
D10		0R0	0B0	1G0	…	158R0	158B0	159G0
D9								
D8								
D7	C7	0G5	1R5	1B5	…	158G5	159R5	159B5
D6	C6	0G4	1R4	1B4	…	158G4	159R4	159B4
D5	C5	0G3	1R3	1B3	…	158G3	159R3	159B3
D4	C4	0G2	1R2	1B2	…	158G2	159R2	159B2
D3	C3	0G1	1R1	1B1	…	158G1	159R1	159B1
D2	C2	0G0	1R0	1B0	…	158G0	159R0	159B0
D1	C1							
D0	C0							

2)MDT[1:0]="01"

Table19.

Count	0	1	2	3		…	317	318	319	320
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B5	1R5	1B5	…	158R5	158B5	159R5	159B5
D14		0R4	0B4	1R4	1B4	…	158R4	158B4	159R4	159B4
D13		0R3	0B3	1R3	1B3	…	158R3	158B3	159R3	159B3
D12		0R2	0B2	1R2	1B2	…	158R2	158B2	159R2	159B2
D11		0R1	0B1	1R1	1B1	…	158R1	158B1	159R1	159B1
D10		0R0	0B0	1R0	1B0	…	158R0	158B0	159R0	159B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	158G5		159G5	
D6	C6	0G4		1G4		…	158G4		159G4	
D5	C5	0G3		1G3		…	158G3		159G3	
D4	C4	0G2		1G2		…	158G2		159G2	
D3	C3	0G1		1G1		…	158G1		159G1	
D2	C2	0G0		1G0		…	158G0		159G0	
D1	C1					…				
D0	C0					…				

3)MDT[1:0]="10"

Table20.

Count	0	1	2	3		…	317	318	319	320
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B1	1R5	1B1	…	158R5	158B1	159R5	159B1
D14		0R4	0B0	1R4	1B0	…	158R4	158B0	159R4	159B0
D13		0R3		1R3		…	158R3		159R3	
D12		0R2		1R2		…	158R2		159R2	
D11		0R1		1R1		…	158R1		159R1	
D10		0R0		1R0		…	158R0		159R0	
D9		0G5		1G5		…	158G5		159G5	
D8		0G4		1G4		…	158G4		159G4	
D7	C7	0G3		1G3		…	158G3		159G3	
D6	C6	0G2		1G2		…	158G2		159G2	
D5	C5	0G1		1G1		…	158G1		159G1	
D4	C4	0G0		1G0		…	158G0		159G0	
D3	C3	0B5		1B5		…	158B5		159B5	
D2	C2	0B4		1B4		…	158B4		159B4	
D1	C1	0B3		1B3		…	158B3		159B3	
D0	C0	0B2		1B2		…	158B2		159B2	

4)MDT[1:0]="11"

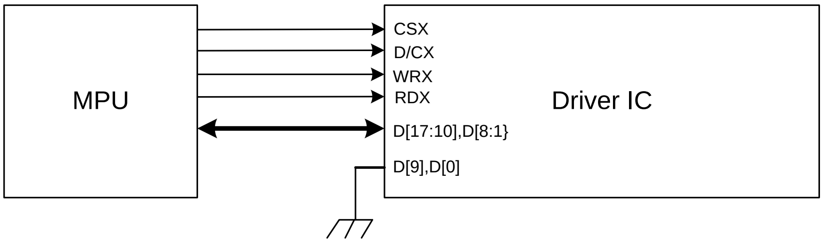
Table21.

Count	0	1	2	3		…	317	318	319	320
D/CX	0	1	1	1		…	1	1	1	1
D15			0R3		1R3	…		158R3		159R3
D14			0R2		1R2	…		158R2		159R2
D13			0R1		1R1	…		158R1		159R1
D12			0R0		1R0	…		158R0		159R0
D11			0G5		1G5	…		158G5		159G5
D10			0G4		1G4	…		158G4		159G4
D9			0G3		1G3	…		158G3		159G3
D8			0G2		1G2	…		158G2		159G2
D7	C7		0G1		1G1	…		158G1		159G1
D6	C6		0G0		1G0	…		158G0		159G0
D5	C5		0B5		1B5	…		158B5		159B5
D4	C4		0B4		1B4	…		158B4		159B4
D3	C3		0B3		1B3	…		158B3		159B3
D2	C2		0B2		1B2	…		158B2		159B2
D1	C1	0R5	0B1	1R5	1B1	…	158R5	158B1	159R5	159B1

D0	C0	0R4	0B0	1R4	1B0	…	158R4	158B0	159R4	159B0

The 8080-II system 16-bit parallel bus interface of GC9D01N can be selected by settings IM [3:0] ="0010". The following shown figure is the example of interface with 8080- MCU system interface.

Figure58.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table22.

Count	0	1	2	3	…	158	159	160
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	157R4	158R4	159R4
D16		0R3	1R3	2R3	…	157R3	158R3	159R3
D15		0R2	1R2	2R2	…	157R2	158R2	159R2
D14		0R1	1R1	2R1	…	157R1	158R1	159R1
D13		0R0	1R0	2R0	…	157R0	158R0	159R0
D12		0G5	1G5	2G5	…	157G5	158G5	159G5
D11		0G4	1G4	2G4	…	157G4	158G4	159G4
D10		0G3	1G3	2G3	…	157G3	158G3	159G3
D8	C7	0G2	1G2	2G2	…	157G2	158G2	159G2
D7	C6	0G1	1G1	2G1	…	157G1	158G1	159G1
D6	C5	0G0	1G0	2G0	…	157G0	158G0	159G0
D5	C4	0B4	1B4	2B4	…	157B4	158B4	159B4
D4	C3	0B3	1B3	2B3	…	157B3	158B3	159B3
D3	C2	0B2	1B2	2B2	…	157B2	158B2	159B2
D2	C1	0B1	1B1	2B1	…	157B1	158B1	159B1
D1	C0	0B0	1B0	2B0	…	157B0	158B0	159B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

1)MDT[1:0]=00

Table23.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	0B5	1G5	…	158R5	158B5	159G5
D16		0R4	0B4	1G4	…	158R4	158B4	159G4
D15		0R3	0B3	1G3	…	158R3	158B3	159G3
D14		0R2	0B2	1G2	…	158R2	158B2	159G2
D13		0R1	0B1	1G1	…	158R1	158B1	159G1
D12		0R0	0B0	1G0	…	158R0	158B0	159G0
D11								
D10								
D8	C7	0G5	1R5	1B5	…	158G5	159R5	159B5
D7	C6	0G4	1R4	1B4	…	158G4	159R4	159B4
D6	C5	0G3	1R3	1B3	…	158G3	159R3	159B3
D5	C4	0G2	1R2	1B2	…	158G2	159R2	159B2
D4	C3	0G1	1R1	1B1	…	158G1	159R1	159B1
D3	C2	0G0	1R0	1B0	…	158G0	159R0	159B0
D2	C1							
D1	C0							

2)MDT[1:0]=01

Table24.

Count	0	1	2	3		…	317	318	719	320
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B5	1R5	1B5	…	158R5	158B5	159R5	159B5
D16		0R4	0B4	1R4	1B4	…	158R4	158B4	159R4	159B4
D15		0R3	0B3	1R3	1B3	…	158R3	158B3	159R3	159B3
D14		0R2	0B2	1R2	1B2	…	158R2	158B2	159R2	159B2
D13		0R1	0B1	1R1	1B1	…	158R1	158B1	159R1	159B1
D12		0R0	0B0	1R0	1B0	…	158R0	158B0	159R0	159B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	158G5		159G5	
D7	C6	0G4		1G4		…	158G4		159G4	
D6	C5	0G3		1G3		…	158G3		159G3	
D5	C4	0G2		1G2		…	158G2		159G2	
D4	C3	0G1		1G1		…	158G1		159G1	
D3	C2	0G0		1G0		…	158G0		159G0	
D2	C1					…				

D1	C0					…				

3)MDT[1:0]=10

Table25.

Count	0	1	2	3		…	317	318	319	320
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B1	1R5	1B1	…	158R5	158B1	159R5	159B1
D16		0R4	0B0	1R4	1B0	…	158R4	158B0	159R4	159B0
D15		0R3		1R3		…	158R3		159R3	
D14		0R2		1R2		…	158R2		159R2	
D13		0R1		1R1		…	158R1		159R1	
D12		0R0		1R0		…	158R0		159R0	
D11		0G5		1G5		…	158G5		159G5	
D10		0G4		1G4		…	158G4		159G4	
D8	C7	0G3		1G3		…	158G3		159G3	
D7	C6	0G2		1G2		…	158G2		159G2	
D6	C5	0G1		1G1		…	158G1		159G1	
D5	C4	0G0		1G0		…	158G0		159G0	
D4	C3	0B5		1B5		…	158B5		159B5	
D3	C2	0B4		1B4		…	158B4		159B4	
D2	C1	0B3		1B3		…	158B3		159B3	
D1	C0	0B2		1B2		…	158B2		159B2	

4)MDT[1:0]=11

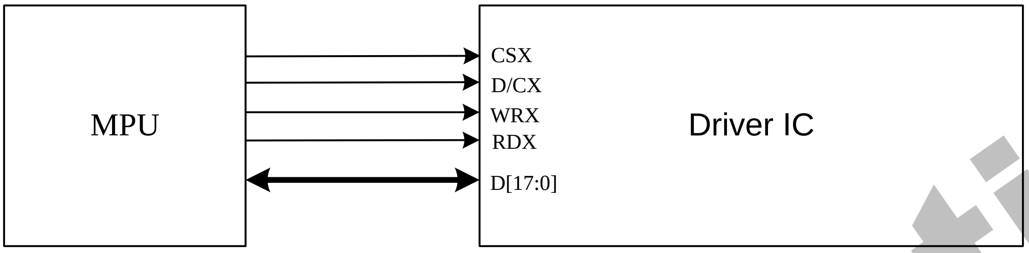
Table26.

Count	0	1	2	3		…	317	318	319	320
D/CX	0	1	1	1		…	1	1	1	1
D17			0R3		1R3	…		158R3		159R3
D16			0R2		1R2	…		158R2		159R2
D15			0R1		1R1	…		158R1		159R1
D14			0R0		1R0	…		158R0		159R0
D13			0G5		1G5	…		158G5		159G5
D12			0G4		1G4	…		158G4		159G4
D11			0G3		1G3	…		158G3		159G3
D10			0G2		1G2	…		158G2		159G2
D8	C7		0G1		1G1	…		158G1		159G1
D7	C6		0G0		1G0	…		158G0		159G0
D6	C5		0B5		1B5	…		358B5		159B5
D5	C4		0B4		1B4	…		358B4		159B4
D4	C3		0B3		1B3	…		358B3		159B3
D3	C2		0B2		1B2	…		358B2		159B2
D2	C1	0R5	0B1	1R5	1B1	…	158R5	358B1	159R5	159B1
D1	C0	0R4	0B0	1R4	1B0	…	158R4	358B0	159R4	159B0

2.4.7. 18-bit Parallel MCU Interface

The 8080-I system 18-bit parallel bus interface I of GC9D01N can be selected by setting hardware pin IM[3:0] to “0111”.The following shown figure is the example of interface with 8080-I MCU system interface.

Figure58.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table27.

Count	0	1	2	3	…	158	159	160
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	157R4	158R4	159R4
D14		0R3	1R3	2R3	…	157R3	158R3	159R3
D13		0R2	1R2	2R2	…	157R2	158R2	159R2
D12		0R1	1R1	2R1	…	157R1	158R1	159R1
D11		0R0	1R0	2R0	…	157R0	158R0	159R0
D10		0G5	1G5	2G5	…	157G5	158G5	159G5
D9		0G4	1G4	2G4	…	157G4	158G4	159G4
D8		0G3	1G3	2G3	…	157G3	158G3	159G3
D7	C7	0G2	1G2	2G2	…	157G2	158G2	159G2
D6	C6	0G1	1G1	2G1	…	157G1	158G1	159G1
D5	C5	0G0	1G0	2G0	…	157G0	158G0	159G0
D4	C4	0B4	1B4	2B4	…	157B4	158B4	159B4
D3	C3	0B3	1B3	2B3	…	157B3	158B3	159B3
D2	C2	0B2	1B2	2B2	…	157B2	158B2	159B2
D1	C1	0B1	1B1	2B1	…	157B1	158B1	159B1
D0	C0	0B0	1B0	2B0	…	157B0	158B0	159B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

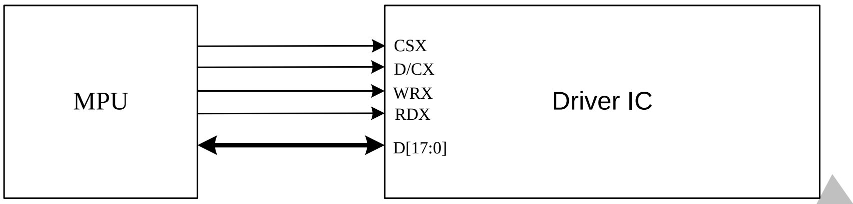
Table28.

Count	0	1	2	3	…	158	159	160
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	157R5	158R5	159R5
D16		0R4	1R4	2R4	…	157R4	158R4	159R4
D15		0R3	1R3	2R3	…	157R3	158R3	159R3
D14		0R2	1R2	2R2	…	157R2	158R2	159R2
D13		0R1	1R1	2R1	…	157R1	158R1	159R1
D12		0R0	1R0	2R0	…	157R0	158R0	159R0
D11		0G5	1G5	2G5	…	157G5	158G5	159G5
D10		0G4	1G4	2G4	…	157G4	158G4	159G4
D9		0G3	1G3	2G3	…	157G3	158G3	159G3
D8		0G2	1G2	2G2	…	157G2	158G2	159G2
D7	C7	0G1	1G1	2G1	…	157G1	158G1	159G1
D6	C6	0G0	1G0	2G0	…	157G0	158G0	159G0
D5	C5	0B5	1B5	2B5	…	157B5	158B5	159B5
D4	C4	0B4	1B4	2B4	…	157B4	158B4	159B4

D3	**C3**	**0B3**	**1B3**	**2B3**	**…**	**157B3**	**158B3**	**159B3**
D2	**C2**	**0B2**	**1B2**	**2B2**	**…**	**157B2**	**158B2**	**159B2**
D1	**C1**	**0B1**	**1B1**	**2B1**	**…**	**157B1**	**158B1**	**159B1**
D0	**C0**	**0B0**	**1B0**	**2B0**	**…**	**157B0**	**158B0**	**159B0**

The 8080-II system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="0011". The following shown figure is the example of interface with 8080- MCU system interface.

Figure59.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table29.

Count	0	1	2	3	…	158	159	160
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	157R4	158R4	159R4
D14		0R3	1R3	2R3	…	157R3	158R3	159R3
D13		0R2	1R2	2R2	…	157R2	158R2	159R2
D12		0R1	1R1	2R1	…	157R1	158R1	159R1
D11		0R0	1R0	2R0	…	157R0	158R0	159R0
D10		0G5	1G5	2G5	…	157G5	158G5	159G5
D9		0G4	1G4	2G4	…	157G4	158G4	159G4
D8	C7	0G3	1G3	2G3	…	157G3	158G3	159G3
D7	C6	0G2	1G2	2G2	…	157G2	158G2	159G2
D6	C5	0G1	1G1	2G1	…	157G1	158G1	159G1
D5	C4	0G0	1G0	2G0	…	157G0	158G0	159G0
D4	C3	0B4	1B4	2B4	…	157B4	158B4	159B4
D3	C2	0B3	1B3	2B3	…	157B3	158B3	159B3
D2	C1	0B2	1B2	2B2	…	157B2	158B2	159B2
D1	C0	0B1	1B1	2B1	…	157B1	158B1	159B1
D0		0B0	1B0	2B0	…	157B0	158B0	159B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table30.

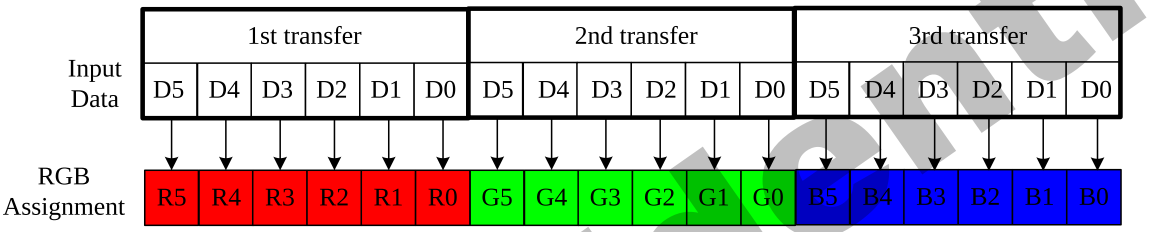
Count	0	1	2	3	…	158	159	160
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	157R5	158R5	159R5
D16		0R4	1R4	2R4	…	157R4	158R4	159R4
D15		0R3	1R3	2R3	…	157R3	158R3	159R3
D14		0R2	1R2	2R2	…	157R2	158R2	159R2
D13		0R1	1R1	2R1	…	157R1	158R1	159R1
D12		0R0	1R0	2R0	…	157R0	158R0	159R0
D11		0G5	1G5	2G5	…	157G5	158G5	159G5
D10		0G4	1G4	2G4	…	157G4	158G4	159G4
D9		0G3	1G3	2G3	…	157G3	158G3	159G3
D8	C7	0G2	1G2	2G2	…	157G2	158G2	159G2
D7	C6	0G1	1G1	2G1	…	157G1	158G1	159G1

D6	C5	0G0	1G0	2G0	…	157G0	158G0	159G0
D5	C4	0B5	1B5	2B5	…	157B5	158B5	159B5
D4	C3	0B4	1B4	2B4	…	157B4	158B4	159B4
D3	C2	0B3	1B3	2B3	…	157B3	158B3	159B3
D2	C1	0B2	1B2	2B2	…	157B2	158B2	159B2
D1	C0	0B1	1B1	2B1	…	157B1	158B1	159B1
D0		0B0	1B0	2B0	…	157B0	158B0	159B0

2.4.8. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the RIM bit to “1”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

1)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).
Figure60.


1st transfer
2nd transfer
3rd transfer
Input Data
D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0
RGB Assignment
R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B5 B4 B3 B2 B1 B0

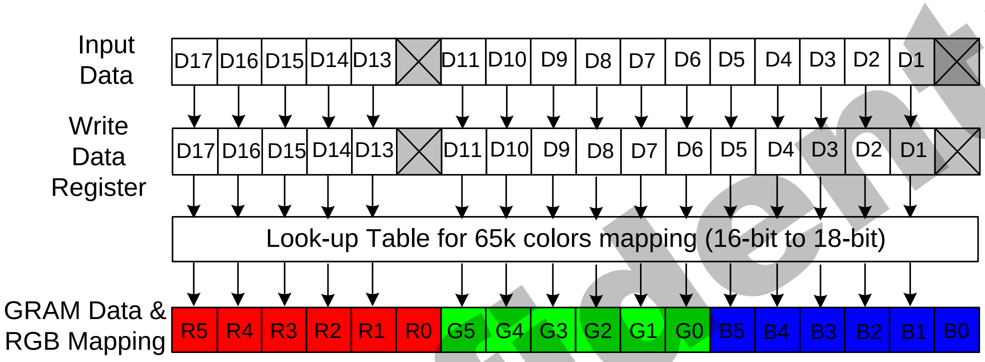
GC9D01N has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK).Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

2.4.9. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D[17:13] & D[11:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:13] & D[11:0] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.

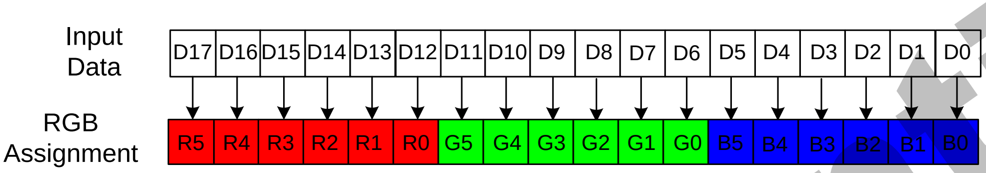
Figure62.


Input Data
D17
D16
D15
D14
D13
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
Write Data Register
Look-up Table for 65k colors mapping (16-bit to 18-bit)
GRAM Data & RGB Mapping
R5
R4
R3
R2
R1
R0
G5
G4
G3
G2
G1
G0
B5
B4
B3
B2
B1
B0

2.4.10. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.

Figure63.



Input Data	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

3. Function Description

3.1. Display data GRAM mapping

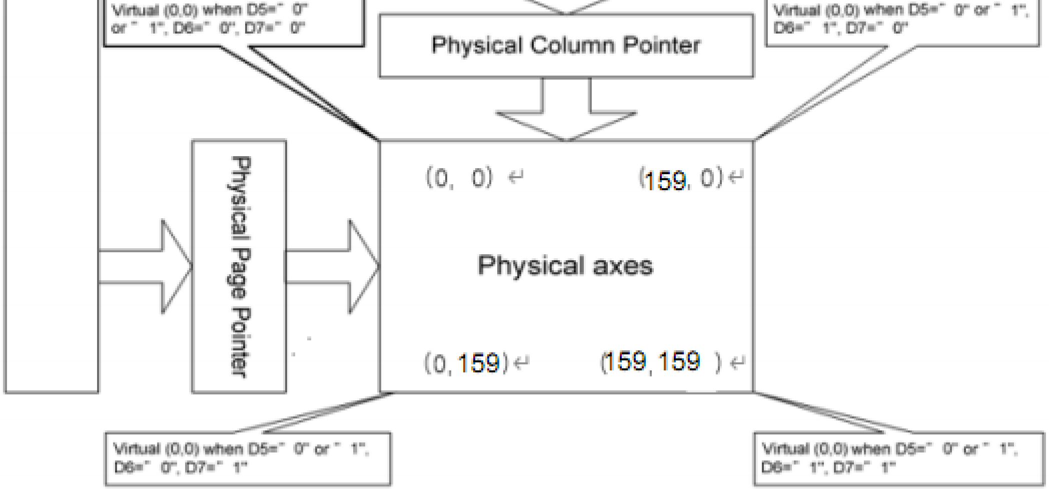
The display data RAM stores display dots and consists of 160x160x18 bits. There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

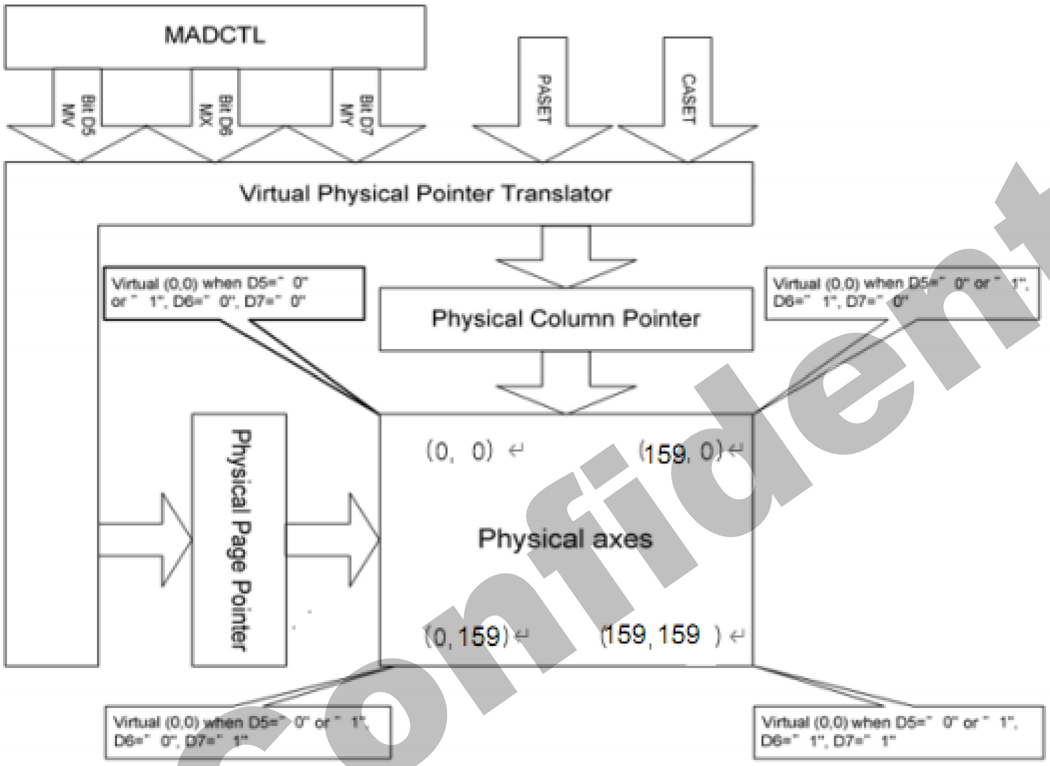
GRAM address for display panel position as shown in the following table

Table31.

(00,00)h	(00,01)h	…… …	(00, 9D)h	(00, 9E)h	(00,9F)h
(01,00)h	(01,01)h	…… …	(01, 9D)h	(01, 9E)h	(01, 9F)h
(02,00)h	(02,01)h	…… …	(02, 9D)h	(02, 9E)h	(02, 9F)h
(03,00)h	(03,01)h	…… …	(03, 9D)h	(03, 9E)h	(03, 9F)h
. . .	. . .	. . .	. . .	. . .	. . .
(9D,00)h	(9D,01)h	…… …	(9D,9D)h	(9D, 9E)h	(9D, 9E)h
(9E,00)h	(9E,01)h	…… …	(9E,9E)h	(9E, 9E)h	(9E, 9E)h
(9F,00)h	(9F,01)h	…… …	(9F,9F)h	(9F, 9F)h	(9F, 9F)h


Virtual (0,0) when D5=" 0" or " 1", D6=" 0", D7=" 0"
Physical Column Pointer
Virtual (0,0) when D5=" 0" or " 1", D6=" 1", D7=" 0"
Physical Page Pointer
(0, 0)
(159, 0)
Physical axes
(0, 159)
(159, 159)
Virtual (0,0) when D5=" 0" or " 1", D6=" 0", D7=" 1"
Virtual (0,0) when D5=" 0" or " 1", D6=" 1", D7=" 1"

by “Memory

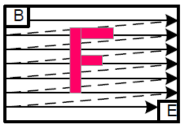
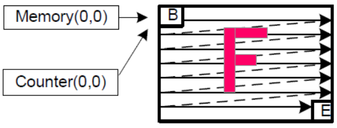
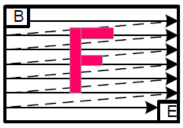
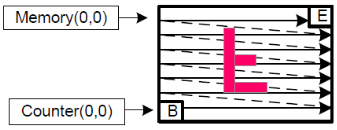
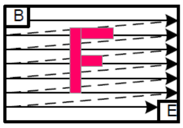
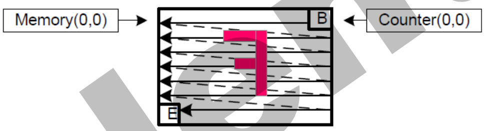
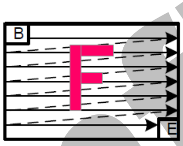
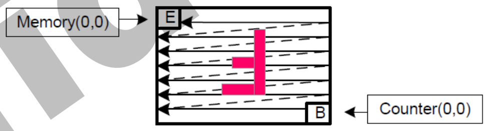
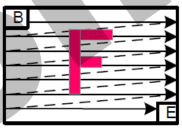
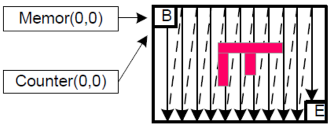
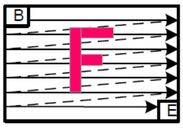
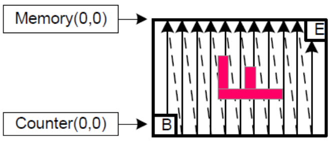
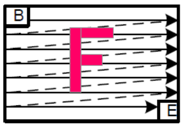
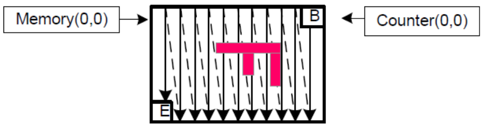
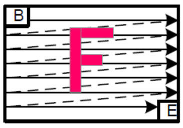
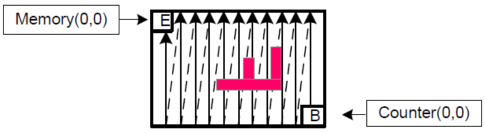

MADCTL
Bit D5 MV
Bit D6 MX
Bit D7 MY
PASET
CASET
Virtual Physical Pointer Translator
Virtual (0,0) when D5=" 0" or " 1", D6=" 0", D7=" 0"
Physical Column Pointer
Virtual (0,0) when D5=" 0" or " 1", D6=" 1", D7=" 0"
Physical Page Pointer
(0, 0)
(159, 0)
Physical axes
(0, 159)
(159, 159)
Virtual (0,0) when D5=" 0" or " 1", D6=" 0", D7=" 1"
Virtual (0,0) when D5=" 0" or " 1", D6=" 1", D7=" 1"

D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159-Physical Page Pointer)
0	1	0	Direct to (159-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (159-Physical Column Pointer)	Direct to (159-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (159-Physical Column Pointer)
1	1	1	Direct to (159-Physical Page Pointer)	Direct to (159-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		 Memory(0,0) Counter(0,0) B E
Y-Mirror	0	0	1		 Memory(0,0) E Counter(0,0) B
X-Mirror	0	1	0		 Memory(0,0) B Counter(0,0) E
X-Mirror Y-Mirror	0	1	1		 Memory(0,0) E B Counter(0,0)
X-Y Exchange	1	0	0		 Memor(0,0) Counter(0,0) B E
X-Y Exchange Y-Mirror	1	0	1		 Memory(0,0) E Counter(0,0) B
X-Y Exchange X-Mirror	1	1	0		 Memory(0,0) B Counter(0,0) E
X-Y Exchange X-Mirror Y-Mirror	1	1	1		 Memory(0,0) E B Counter(0,0)

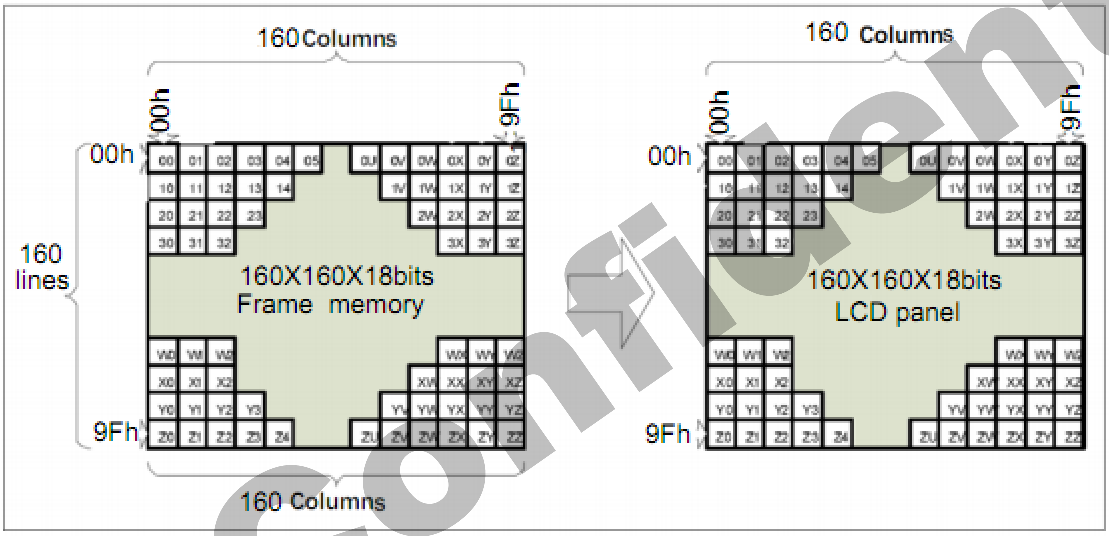
3.3. GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement.

The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

GC9D01N supports three kinds of display mode: one is Normal Display Mode, the other is Partial Display Mode, and Scrolling Display Mode.

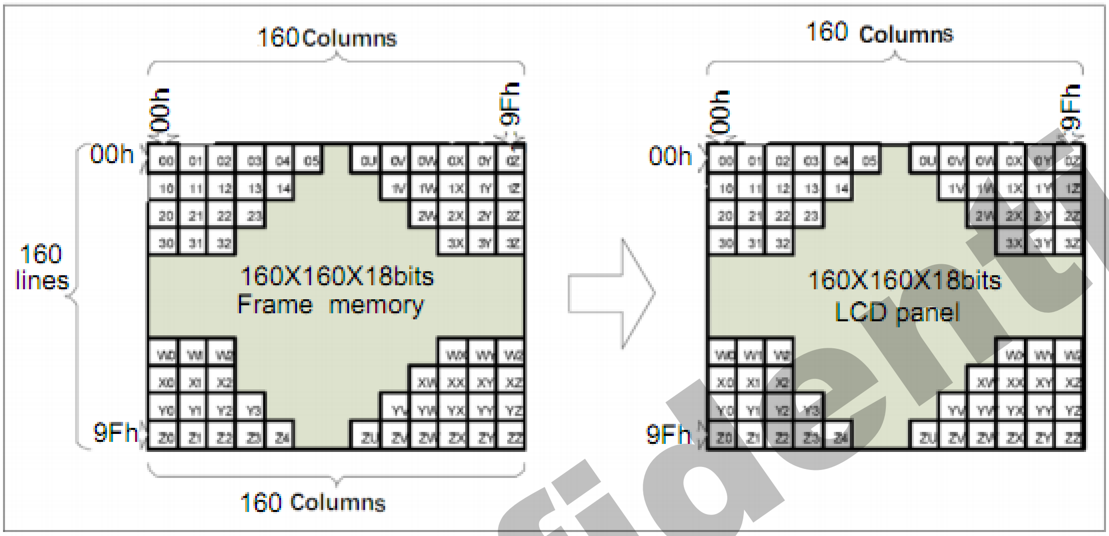

160Columns
00h
9Fh
00h
160
lines
160X160X18bits
Frame memory
9Fh
160 Columns
160 Columns
00h
9Fh
00h
160X160X18bits
LCD panel
9Fh

3.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 0167h and page pointer is 0000h to 0167h is displayed.

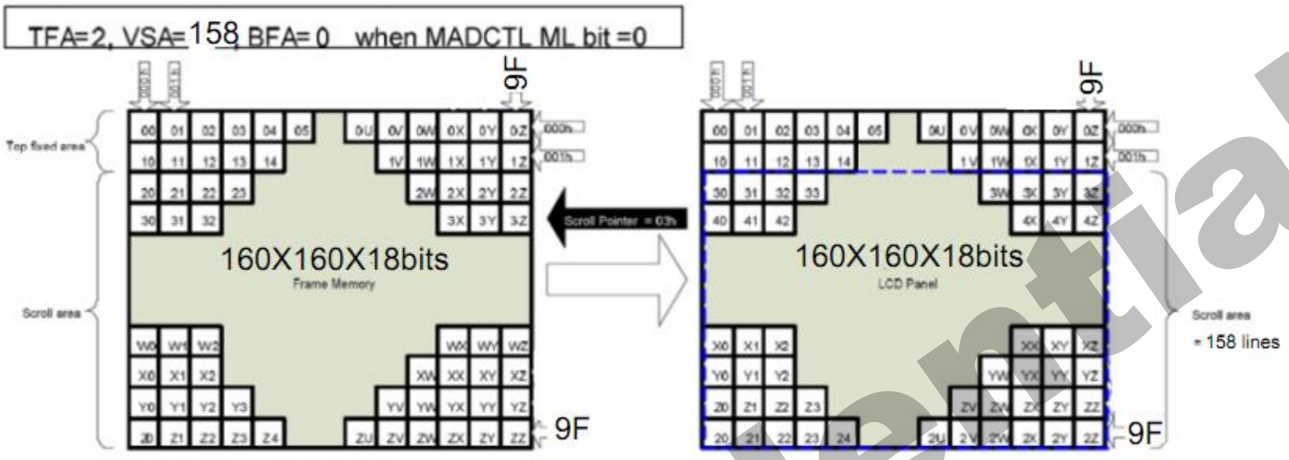
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)

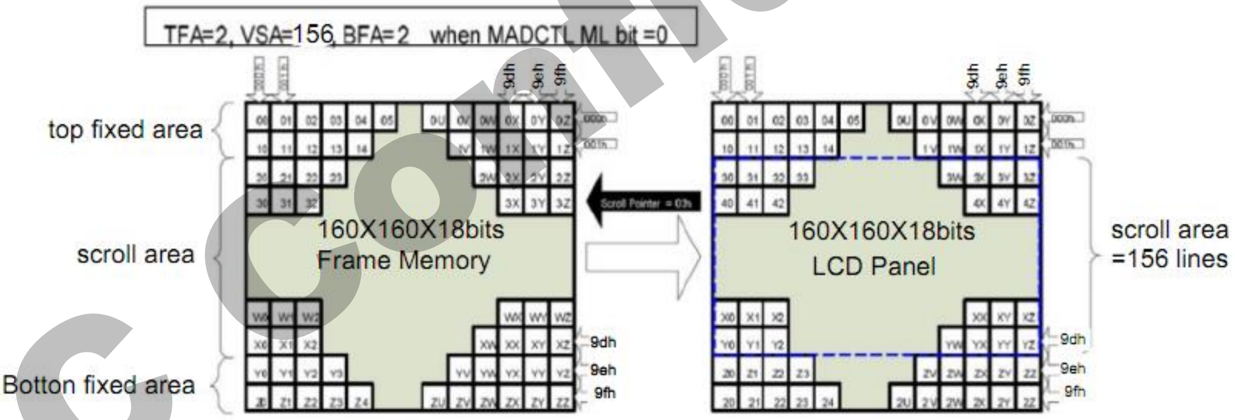
Figure66.

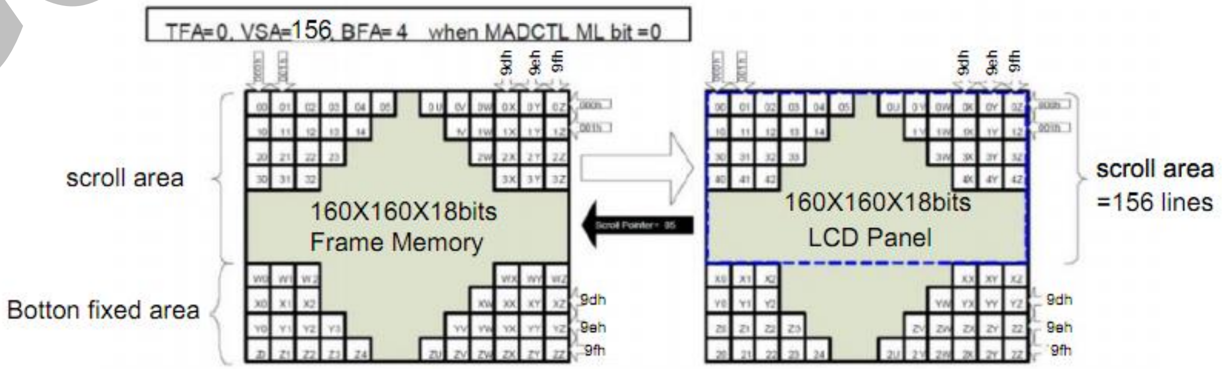

160Columns
00h
9Fh
00h
160 lines
9Fh
160X160X18bits
Frame memory
160 Columns
160 Columns
00h
9Fh
00h
9Fh
160X160X18bits
LCD panel

3.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).


TFA=2, VSA=158 BFA=0 when MADCTL ML bit =0
Top fixed area
Scroll area
160X160X18bits
Frame Memory
Scroll Pointer = 03h
160X160X18bits
LCD Panel
Scroll area
= 158 lines
9F
9F
9F
9F


TFA=2, VSA=156 BFA=2 when MADCTL ML bit =0
top fixed area
scroll area
Botton fixed area
160X160X18bits
Frame Memory
Scroll Pointer = 03h
160X160X18bits
LCD Panel
scroll area
=156 lines
9dh
9eh
9fh


TFA=0, VSA=156 BFA=4 when MADCTL ML bit =0
scroll area
Botton fixed area
160X160X18bits
Frame Memory
Scroll Pointer = 95
160X160X18bits
LCD Panel
scroll area
=156 lines
9dh
9eh
9fh

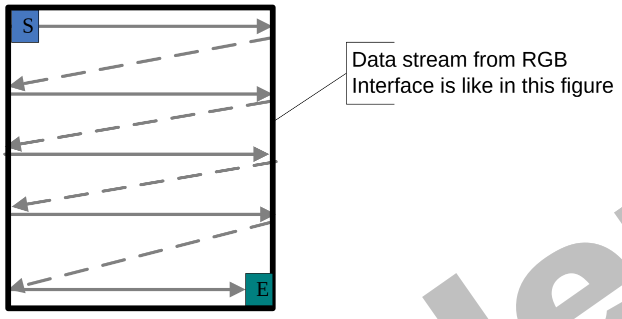
Note: When Vertical Scrolling Definition Parameters(TFA+VSA+BFA) ≠160，scrolling mode is undefined.

3.3.3. Updating order on display active area in RGB interface mode

There is defined different kind of updating orders for display in RGB interface mode (**RCM [1:0]** =’1x’).

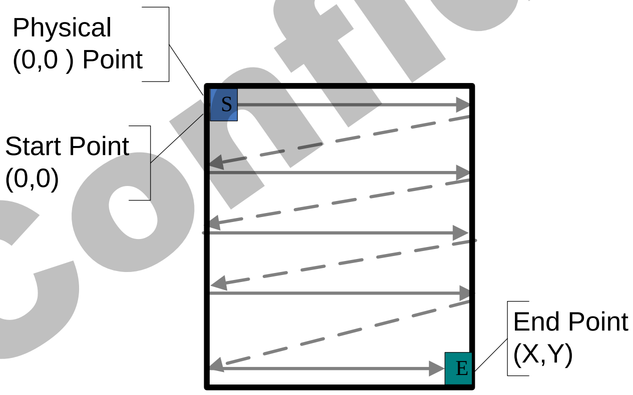
These updating are controlled by **MY** and **MX** bits. Data streaming direction from the host to the display is described in the following figure.

Figure74.


S
E
Data stream from RGB Interface is like in this figure

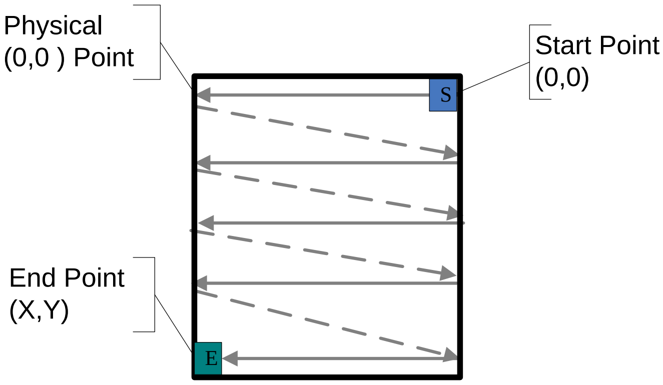
Updating order when MY = ‘0’ and MX = ‘0’

Figure75.


Physical (0,0) Point
Start Point (0,0)
S
E
End Point (X,Y)

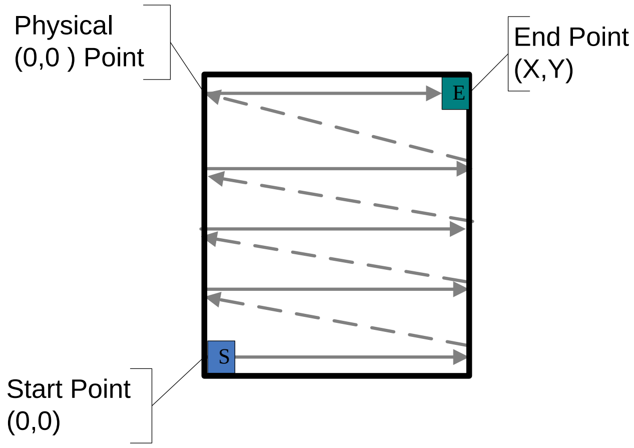
Updating order when MY = ‘0’ and MX = ‘1’

Figure76.


Physical (0,0) Point
Start Point (0,0)
S
End Point (X,Y)
E

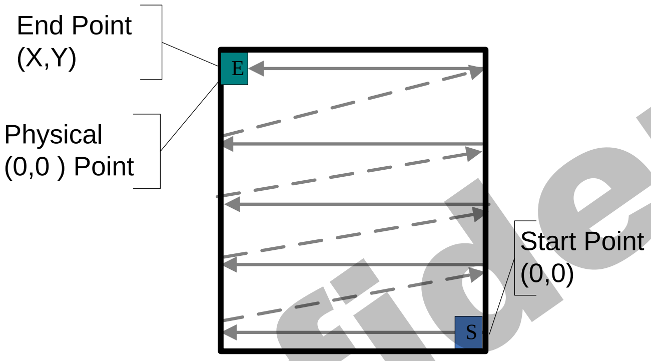
Updating order when MY = ‘1’ and MX = ‘0’

Figure77.


Physical
(0,0) Point
End Point
(X,Y)
E
S
Start Point
(0,0)

Updating order when MY = '1' and MX = '1'

Figure78.


End Point
(X,Y)
Physical
(0,0) Point
E
Start Point
(0,0)
S

Rules for updating order on display active area in RGB interface display mode:

Table37.

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to 0 "Start Column"	Return to "Start Page"

Note: Pixel order is RGB on the display.

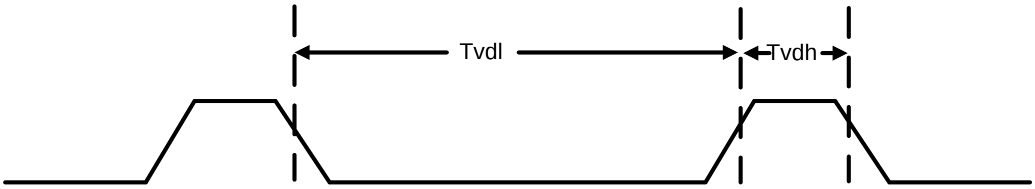
3.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

3.4.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:

Figure79.

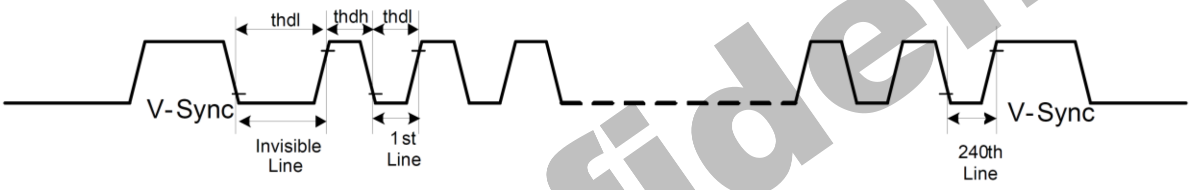


tVdh= The LCD display is not updated from the Frame Memory

tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 160 H-sync pulses per field.

Figure80.


thdl
thdh
thdl
V-Sync
Invisible Line
1 st Line
240th Line
V-Sync

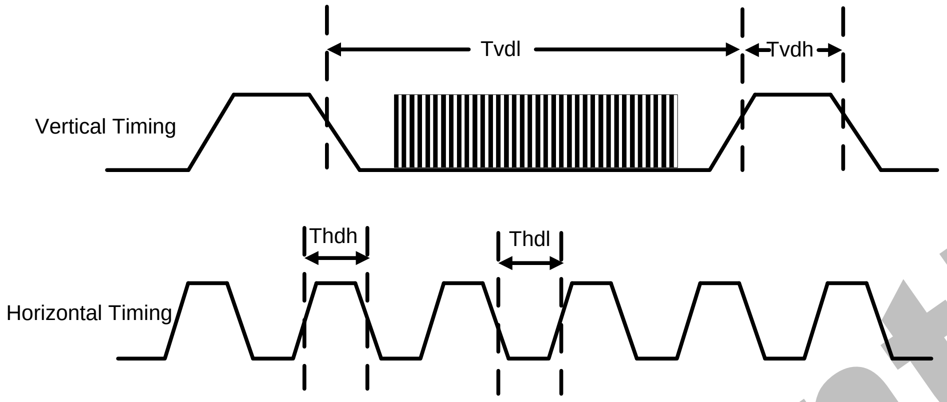
thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

3.4.2. Tearing effect line timing

The Tearing Effect signal is described below.

Figure81.


Tvdl
Tvdh
Vertical Timing
Thdh
Thdl
Horizontal Timing

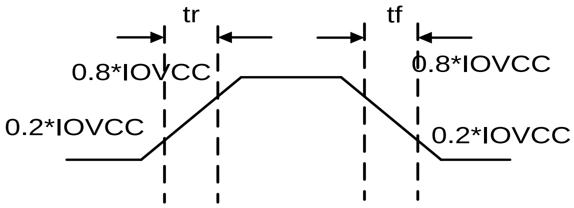
Idle Mode Off (Frame Rate = 20~65 Hz)

Table38.

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 20~65 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Figure82.


tr
tf
0.8*IOVCC
0.2*IOVCC
0.8*IOVCC
0.2*IOVCC

The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

3.5. Source driver

The GC9D01N contains a 240 channels of source driver (S1~S240) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 240 channels and generates corresponding

gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

3.6. Gate driver

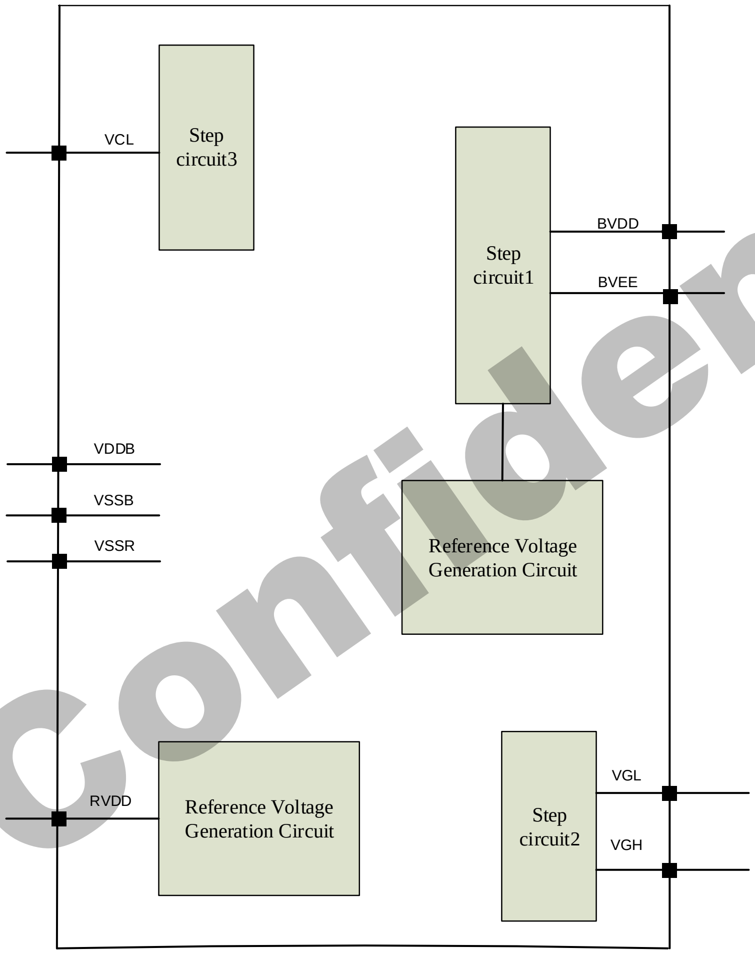
The GC9D01N contains a 32 gate channels of gate driver (G1~G32) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

3.7. LCD power generation circuit

3.7.1. Power supply circuit

The power circuit of GC9D01N is used to generate supply voltages for LCD panel driving.

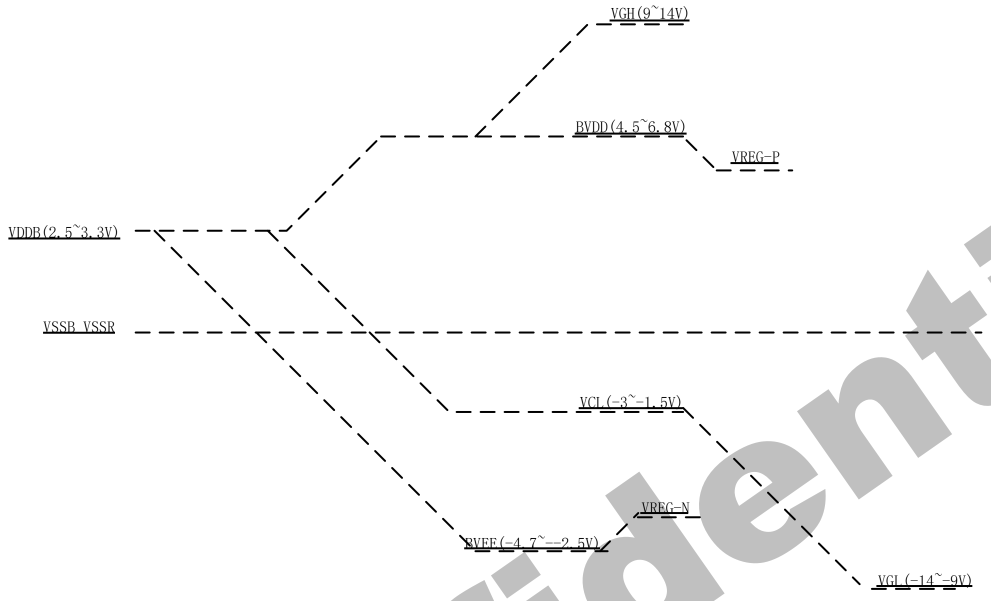
Figure83.


VCL
Step circuit3
Step circuit1
BVDD
BVEE
VDDB
VSSB
VSSR
Reference Voltage Generation Circuit
RVDD
Reference Voltage Generation Circuit
Step circuit2
VGL
VGH

3.7.2. LCD power generation scheme

The boost voltage generated is shown as below.

Figure84.


VGH(9~14V)
BVDD(4.5~6.8V)
VREG-P
VDDB(2.5~3.3V)
VSSB VSSR
VCL(-3~-1.5V)
VREG-N
BVEE(-4.7~--2.5V)
VGL(-14~-9V)

LCD power generation scheme

3.8. Gamma Correction

GC9D01N incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9D01N available with liquid crystal panels of various characteristics.

Figure85.

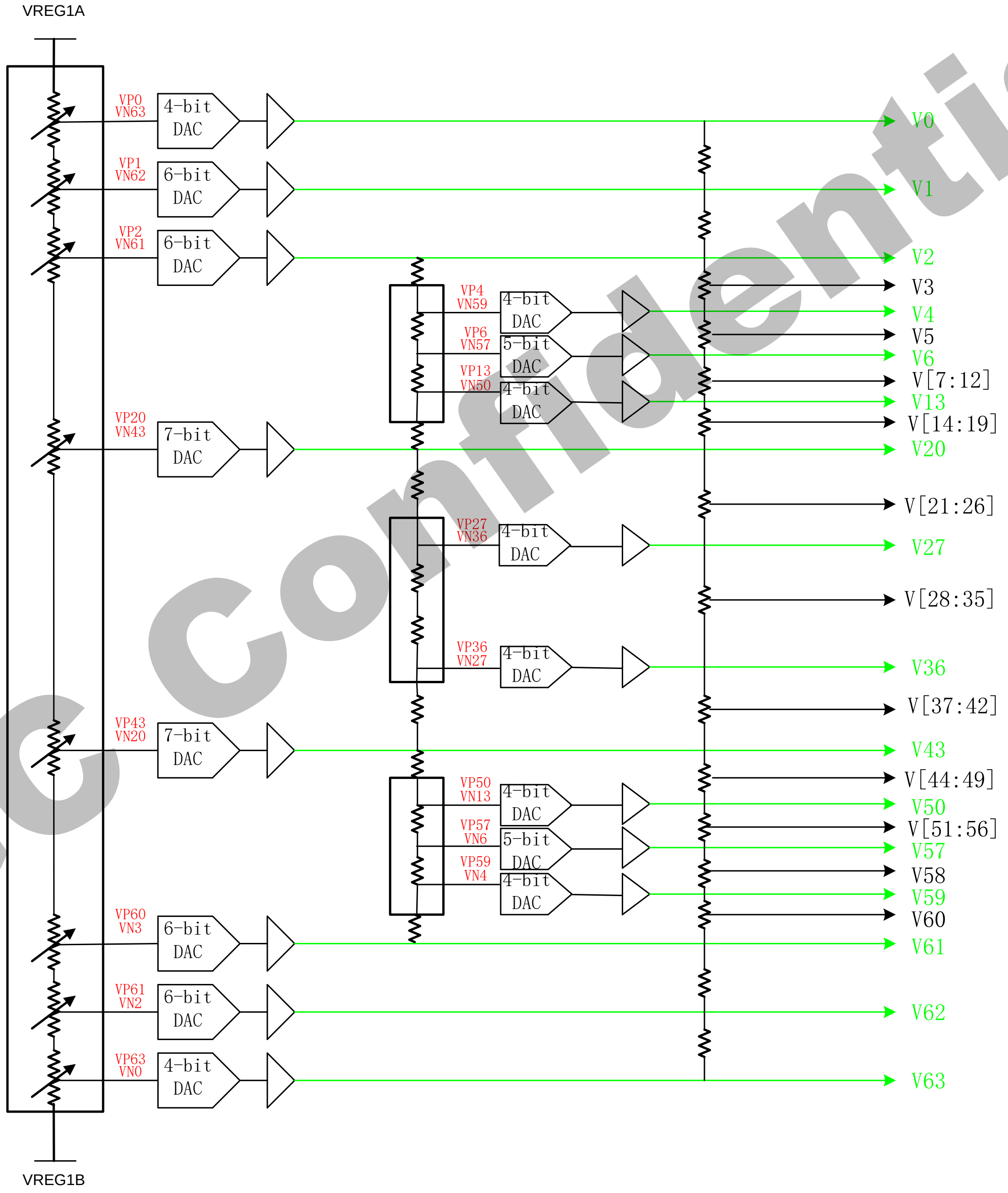
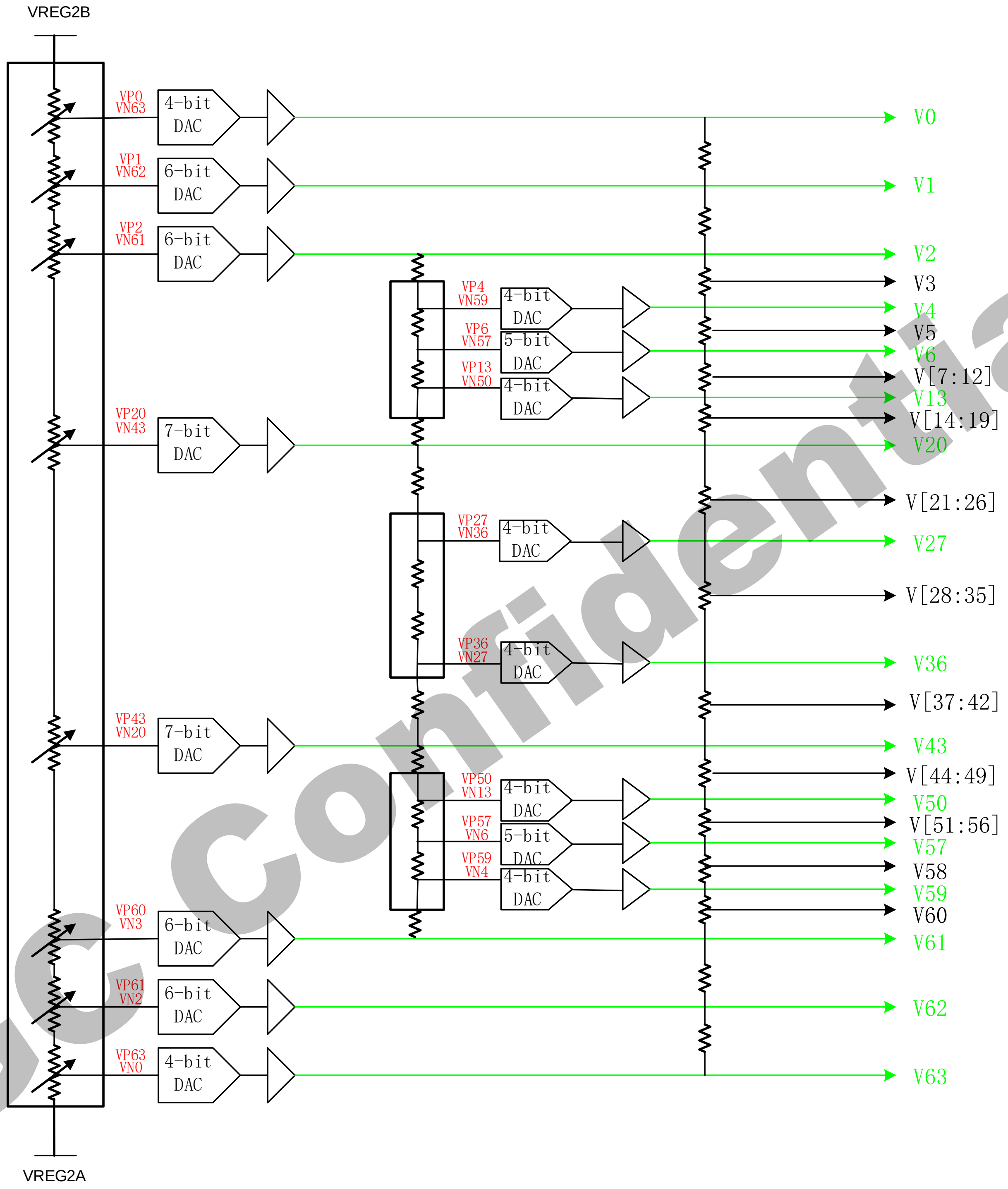
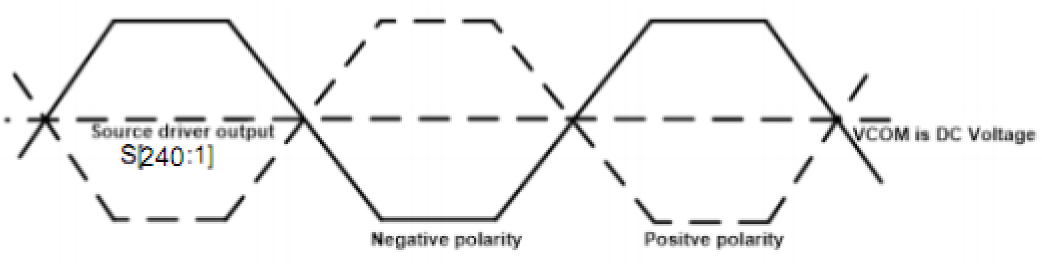

VREG1A
VP0
VN63
4-bit DAC
V0
VP1
VN62
6-bit DAC
V1
VP2
VN61
6-bit DAC
V2
V3
VP4
VN59
4-bit DAC
V4
V5
VP6
VN57
5-bit DAC
V6
VP13
VN50
4-bit DAC
V[7:12]
V13
V[14:19]
VP20
VN43
7-bit DAC
V20
V[21:26]
VP27
VN36
4-bit DAC
V27
V[28:35]
VP36
VN27
4-bit DAC
V36
V[37:42]
VP43
VN20
7-bit DAC
V43
V[44:49]
VP50
VN13
4-bit DAC
V50
V[51:56]
VP57
VN6
5-bit DAC
V57
V58
VP59
VN4
4-bit DAC
V59
V60
VP60
VN3
6-bit DAC
V61
VP61
VN2
6-bit DAC
V62
VP63
VN0
4-bit DAC
V63
VREG1B

Figure86.


VREG2B
VP0
VN63
4-bit
DAC
V0
VP1
VN62
6-bit
DAC
V1
VP2
VN61
6-bit
DAC
V2
V3
VP4
VN59
4-bit
DAC
V4
V5
VP6
VN57
5-bit
DAC
V6
V[7:12]
VP13
VN50
4-bit
DAC
V13
V[14:19]
VP20
VN43
7-bit
DAC
V20
V[21:26]
VP27
VN36
4-bit
DAC
V27
V[28:35]
VP36
VN27
4-bit
DAC
V36
V[37:42]
VP43
VN20
7-bit
DAC
V43
V[44:49]
VP50
VN13
4-bit
DAC
V50
V[51:56]
VP57
VN6
5-bit
DAC
V57
V58
VP59
VN4
4-bit
DAC
V59
V60
VP60
VN3
6-bit
DAC
V61
VP61
VN2
6-bit
DAC
V62
VP63
VN0
4-bit
DAC
V63
VREG2A

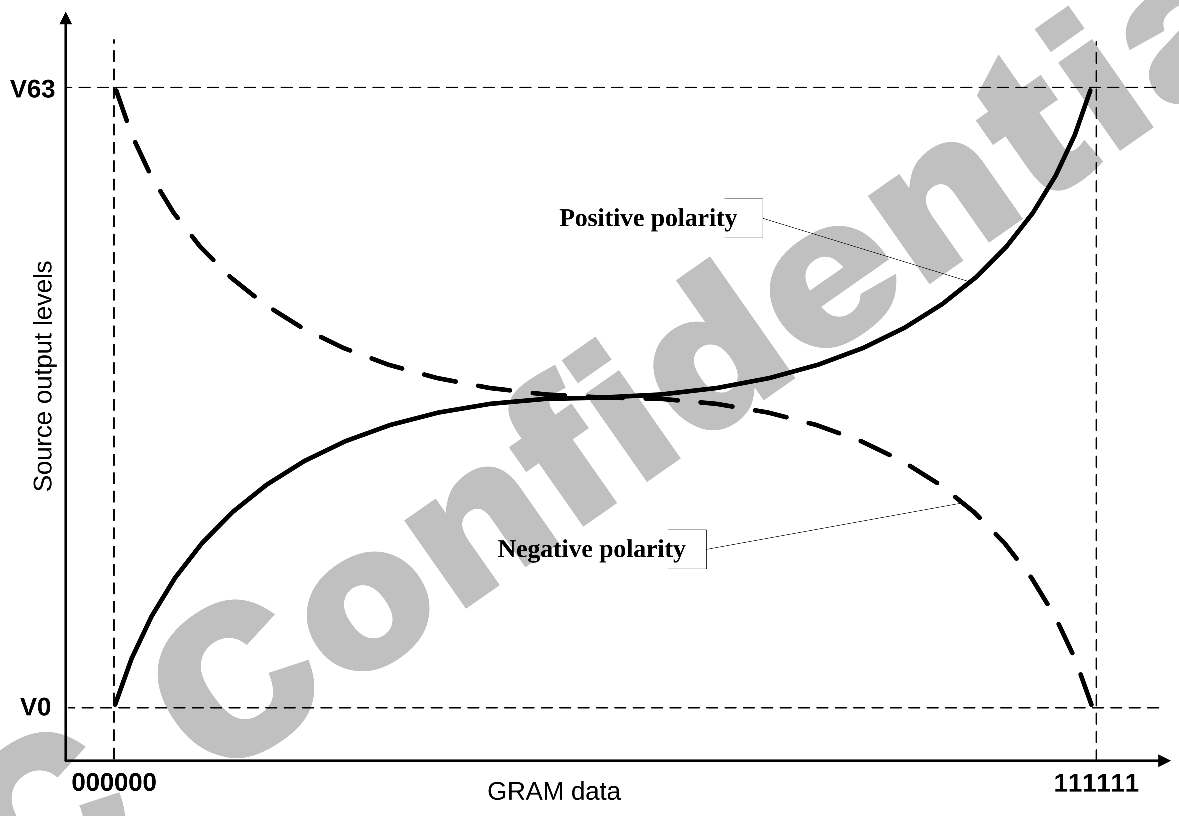
Grayscale Voltage Generation

Figure87.Dot inversion


Source driver output
S[240:1]
VCOM is DC Voltage
Negative polarity
Positve polarity

Relationship between Source Output and VCOM

Figure88.



3.9. Power Level Definition

3.9.1. Power Levels

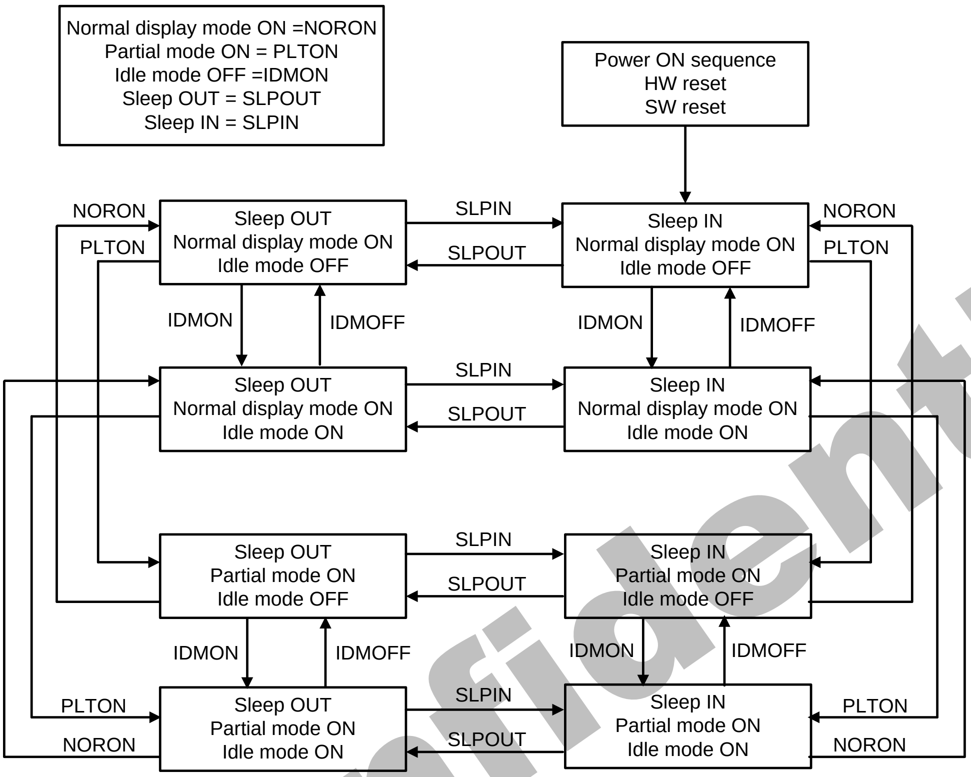
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VDDB and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

3.9.2. Power Flow Chart

Figure89.


Normal display mode ON =NORON
Partial mode ON = PLTON
Idle mode OFF =IDMON
Sleep OUT = SLPOUT
Sleep IN = SLPIN
Power ON sequence
HW reset
SW reset
Sleep OUT
Normal display mode ON
Idle mode OFF
Sleep IN
Normal display mode ON
Idle mode OFF
Sleep OUT
Normal display mode ON
Idle mode ON
Sleep IN
Normal display mode ON
Idle mode ON
Sleep OUT
Partial mode ON
Idle mode OFF
Sleep IN
Partial mode ON
Idle mode OFF
Sleep OUT
Partial mode ON
Idle mode ON
Sleep IN
Partial mode ON
Idle mode ON
SLPIN
SLPOUT
IDMON
IDMOFF
NORON
PLTON

Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

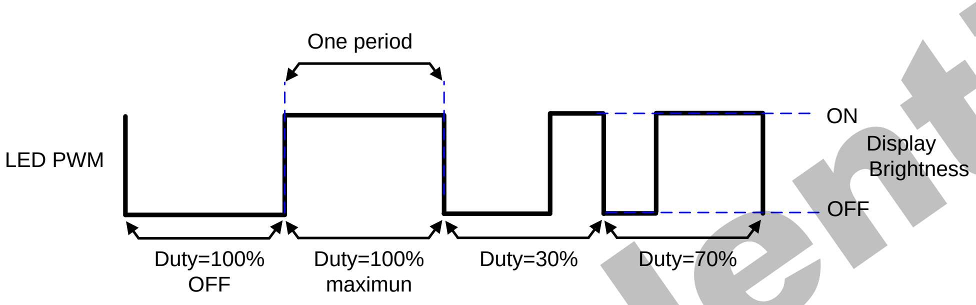
3.10. Brightness control block

There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0]/255 x period (affected by OSC frequency).

For example: LEDPWM period = 3ms, and DBV[7:0] = ‘200DEC’. Then LEDPWM duty = 200 / 255=78.1%. Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344ms, and the low-level of LEDPWM = 0.656ms.

Figure90.


One period
LED PWM
ON
Display Brightness
OFF
Duty=100% OFF
Duty=100% maximun
Duty=30%
Duty=70%

LEDPWM output duty

3.11. Input/output pin state

3.11.1. Output pins

Table40.

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
LEDPWM	Low	Low

Characteristics of output pins

3.11.2. Input pins

Table41.

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
D[17:0]	Input invalid	Input valid	Input valid	Input invalid
IM[3:0]	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

4. Command

4.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID_1[7:0]								00
	1	↑	1	XX	ID_2[7:0]								9D
	1	↑	1	XX	ID_3[7:0]								01
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:25]							X	00
	1	↑	1	XX	X	D[22:20]			D[19:16]				61
	1	↑	1	XX	X	X	X	X	X	D[10:8]			00
	1	↑	1	XX	D[7:5]			X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								00
	1	1	↑	XX	SC[7:0]								00
	1	1	↑	XX	EC[15:8]								01
	1	1	↑	XX	EC[7:0]								67h
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								00

	1	1	↑	XX	SP[7:0]								00
	1	1	↑	XX	EP[15:8]								01h
	1	1	↑	XX	EP[7:0]								67h
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								01
	1	1	↑	XX	ER[7:0]								67
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								01
	1	1	↑	XX	VSA[7:0]								67
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI[2:0]			X	DBI[2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D[17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS[8]	00
	1	1	↑	XX	STS[7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	X	GTS	00

												[8]	
	1	↑	1	XX	GTS[7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								00
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								9D
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								01

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	0	RCM[1:0]		X	VSPL	HSPL	DPL	EPL	01
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	0	0	0	VFP[3:0]				08
	1	1	↑	XX	0	VBP[6:0]							02
	1	1	↑	XX	0	0	0	HBP[4:0]					14
Display Function Control	0	1	1	XX	1	0	1	1	0	1	1	0	B6
	1	1	1	XX	X	X	X	X	X	X	X	X	00
	1	1	1	XX	X	GS	SS	X	X	X	X	X	00
TE Control	0	1	↑	XX	1	0	1	1	1	0	1	0	B4h
	1	1	↑	XX	te_width[7:0]								00
	1	1	↑	XX	X	X	X	X	X	X	X	te_pol	00
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	epf[1:0]		Mdt[1:0]		DM[1:0]		RM	RIM	C0

Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Power Criterion Control	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	0	0	0	0	0	0	vcire	0	00
Vreg1a voltage Control	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XX	0	vreg1_vbp_d[6:0]							3C
Vreg1b voltage Control	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XX	0	vreg1_vbn_d[6:0]							3C
Vreg2a voltage Control	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
	1	1	↑	XX	0	0	vrh[5:0]						28
Inversion	0	1	↑	XX	1	1	1	0	1	1	0	0	ECh
	1	1	↑	XX	x	DINV[2:0]			x	x			77
Dual-Single gate select	0	1	↑	XX	1	0	1	1	1	1	1	1	BFh
	1	1	↑	XX	0	0	0	0	0	0	0	Dual-gate	01

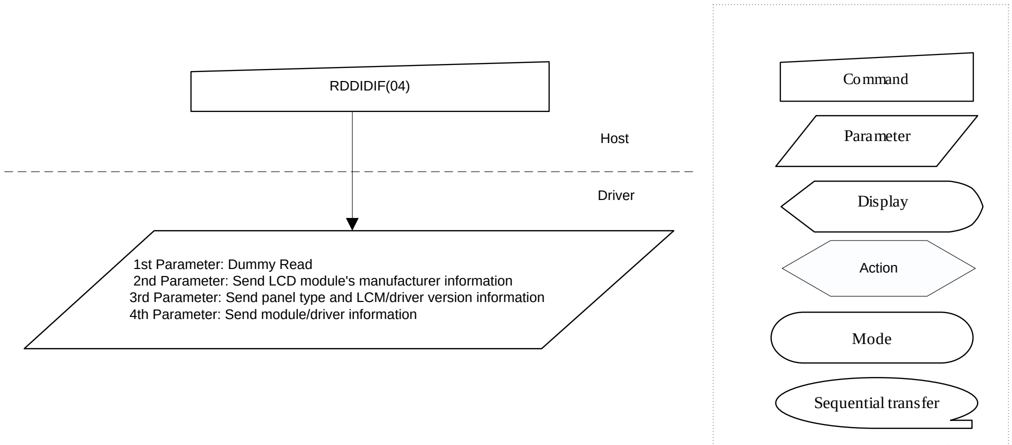
SPI 2data control	0	1	↑	XX	1	1	1	0	1	0	0	1	B1h
	1	1	↑	XX	x	x	x	x	2data_en	2data_mdt			00
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
SET_GAMMA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX	dig2gam_dig2j0_n[1:0]		dig2gam_vr1_n[5:0]						80
	1	1	↑	XX	dig2gam_dig2j1_n[1:0]		dig2gam_vr2_n[5:0]						03
	1	1	↑	XX	0	0	0	dig2gam_vr4_n[4:0]					08
	1	1	↑	XX	0	0	0	dig2gam_vr6_n[4:0]					06
	1	1	↑	XX	dig2gam_vr0_n[3:0]				dig2gam_vr13_n[3:0]				05
	1	1	↑	XX	0	dig2gam_vr20_n[6:0]							2B
SET_GAMMA2	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX	0	dig2gam_vr43_n[6:0]							41
	1	1	↑	XX	dig2gam_vr27_n[2:0]			dig2gam_vr57_n[4:0]					97
	1	1	↑	XX	dig2gam_vr36_n[2:0]			dig2gam_vr59_n[4:0]					98
	1	1	↑	XX	0	0	dig2gam_vr61_n[5:0]						13
	1	1	↑	XX	0	0	dig2gam_vr62_n[5:0]						17
	1	1	↑	XX	dig2gam_vr50_n[3:0]				dig2gam_vr63_n[3:0]				CD
SET_GAMMA3	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	dig2gam_dig2j0_p[1:0]		dig2gam_vr1_p[5:0]						40
	1	1	↑	XX	dig2gam_dig2j1_p[1:0]		dig2gam_vr2_p[5:0]						03
	1	1	↑	XX	0	0	0	dig2gam_vr4_p[4:0]					08
	1	1	↑	XX	0	0	0	dig2gam_vr6_p[4:0]					0B
	1	1	↑	XX	dig2gam_vr0_p[3:0]				dig2gam_vr13_p[3:0]				08
	1	1	↑	XX	0	dig2gam_vr20_p[6:0]							2E
SET_GAMMA4	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h
	1	1	↑	XX	0	dig2gam_vr43_p[6:0]							3F
	1	1	↑	XX	dig2gam_vr27			dig2gam_vr57_p[4:0]					98

					_p[2:0]								
	1	1	↑	XX	dig2gam_vr36_p[2:0]			dig2gam_vr59_p[4:0]					B4
	1	1	↑	XX	0	0	dig2gam_vr61_p[5:0]						14
	1	1	↑	XX	0	0	dig2gam_vr62_p[5:0]						18
	1	1	↑	XX	dig2gam_vr50_p[3:0]				dig2gam_vr63_p[3:0]				CD

4.2. Description of Level 1 Command

4.2.1. Read display identification information (04h)

<table>
<tr><td>04h</td><td colspan="13">Read display identification information 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_1[7:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_2[7:0]</td><td>9C</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_3[7:0]</td><td>01</td></tr>
<tr><td>Description</td><td colspan="13">This read byte returns 24 bits display identification information.
The 1st parameter is dummy data.
The 2nd parameter (ID2_1 [7:0]): LCD module's manufacturer ID.
The 3rd parameter (ID2_2 [7:0]): LCD module/driver version ID.
The 4th parameter (ID2_3 [7:0]): LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>24'h009C01</td></tr>
<tr><td>SW Reset</td><td>24'h009C01</td></tr>
<tr><td>HW Reset</td><td>24'h009C01</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDDIDIF(04)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send LCD module's manufacturer information
3rd Parameter: Send panel type and LCM/driver version information
4th Parameter: Send module/driver information
Command
Parameter
Display
Action
Mode
Sequential transfer

4.2.2. Read Display Status (09h)

09h	Read Display Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D[31:25]							X	00
3rd Parameter	1	↑	1	XX	0	D[22:20]			D[19:16]				61
4th Parameter	1	↑	1	XX	0	0	0	0	0	D[10:8]			00
5th Parameter	1	↑	1	XX	D[7:5]			0	0	0	0	0	00
Description	This command indicates the current status of the display as described in the table below:												

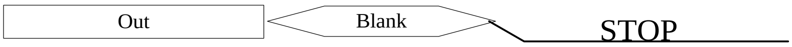
Bit	Description	Value	Status
D31	Booster voltage status	O	Booster OFF
		1	Booster ON
D30	Row address order	O	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	O	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	O	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	O	LCD Refresh Top to BoUom (When MADCTL B4='0')
		1	LCD Refresh BoUom to Top (When MADCTL B4='1').
D26	RGB/BGR order	O	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	O	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When

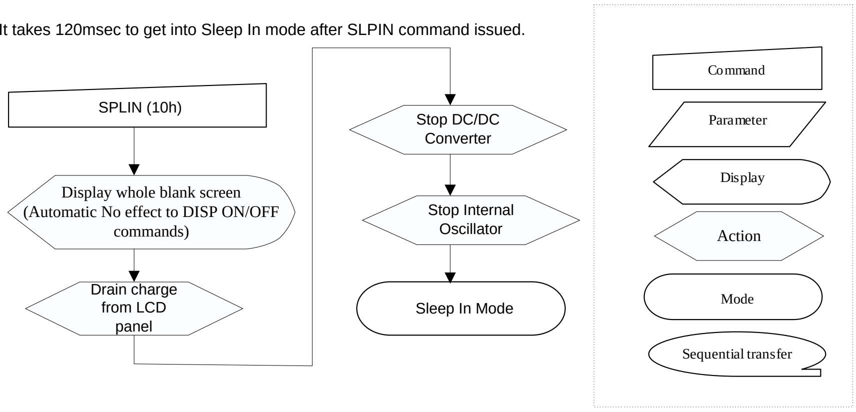
			MADCTL B2='1')
D24	Not used	O	-
D23	Not used	O	-
D22 D21 D20	Interface color pixel format definition	101	16-bit/pixel
		110	18-bit/pixel
D19	Idle mode ON/OFF	O	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	O	Partial Mode OFF
		1	Partial Mode ON
D17	Sleep IN/OUT	O	Sleep IN Mode
		1	Sleep OUT Mode
D16	Display normal mode ON/OFF	O	Display Normal Mode OFF.
		1	Display Normal Mode ON.
D15	Vertical scrolling status	O	Scroll OFF
D14	Not used	O	-
D13	Inversion status	O	Not defined
D12	All pixel ON	O	Not defined
D11	All pixel OFF	O	Not defined
D10	Display ON/OFF	O	
		1	Display is ON
D9	Tearing effect line ON/OFF	O	Tearing Effect Line OFF
		1	Tearing Effect ON
D5	Tearing effect line mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking
D4	Not used	O	-
D3	Not used	O	-
D2	Not used	O	-
D1	Not used	O	-
D0	Not used	O	-

Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

4.2.3. Enter Sleep Mode (10h)

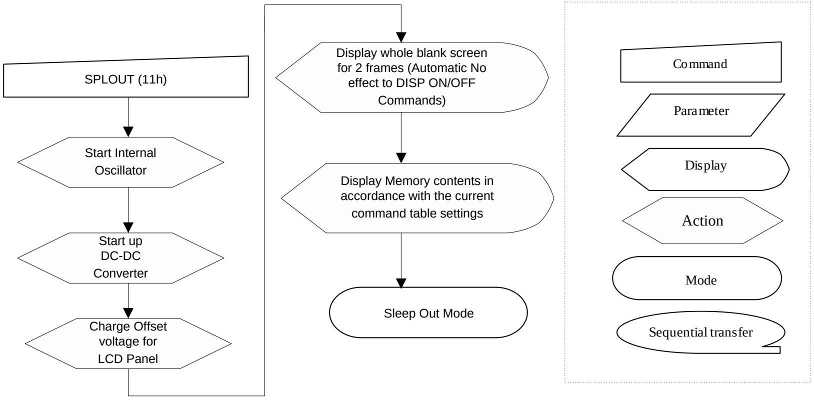
<table>
<tr><th>10h</th><th colspan="12">Enter Sleep Mode</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped

MCU interface and memory are still working and the memory keeps its contents.
X = Don't care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr>
<tr><td>SW Reset</td><td>Sleep IN Mode</td></tr>
<tr><td>HW Reset</td><td>Sleep IN Mode</td></tr>
</table></td></tr>
</table>

Flow Chart	It takes 120msec to get into Sleep In mode after SLPIN command issued. 

SPLIN (10h)
Display whole blank screen (Automatic No effect to DISP ON/OFF commands)
Drain charge from LCD panel
Stop DC/DC Converter
Stop Internal Oscillator
Sleep In Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

4.2.4. Sleep Out Mode (11h)

<table>
<tr><td>11h</td><td colspan="12">Sleep Out Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr>
<tr><td>SW Reset</td><td>Sleep IN Mode</td></tr>
<tr><td>HW Reset</td><td>Sleep IN Mode</td></tr>
</table>
</td></tr>
</table>

Flow Chart	 SPLOUT (11h) Start Internal Oscillator Start up DC-DC Converter Charge Offset voltage for LCD Panel Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands) Display Memory contents in accordance with the current command table settings Sleep Out Mode Command Parameter Display Action Mode Sequential transfer

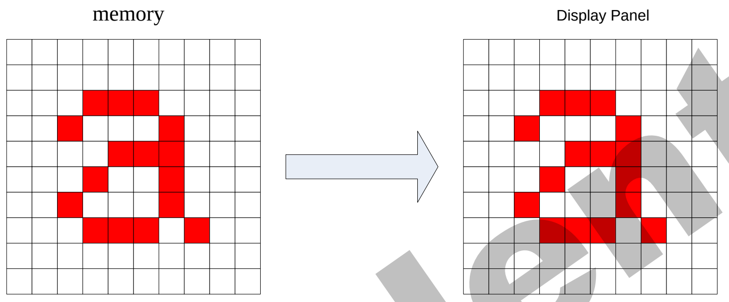
4.2.5. Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="13">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr>
<tr><td>SW Reset</td><td>Normal Display Mode</td></tr>
<tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

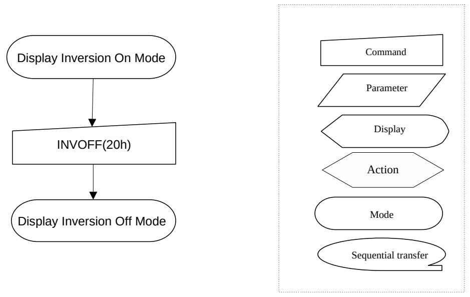
4.2.6. Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="13">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr>
<tr><td>SW Reset</td><td>Normal Display Mode</td></tr>
<tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

4.2.7. Display Inversion OFF (20h)

<table>
<tr><td>20h</td><td colspan="13">Display Inversion OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>20h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from display inversion mode.
This command makes no change of the content of frame memory.
This command doesn’t change any other status.


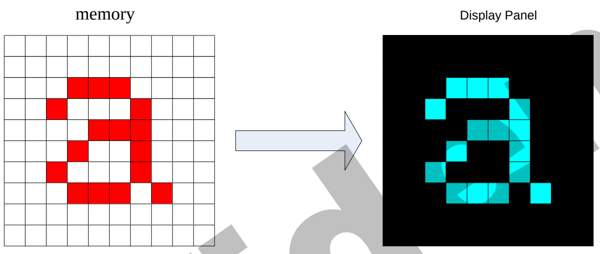
memory
Display Panel

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion OFF mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr>
<tr><td>SW Reset</td><td>Display Inversion OFF</td></tr>
<tr><td>HW Reset</td><td>Display Inversion OFF</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">

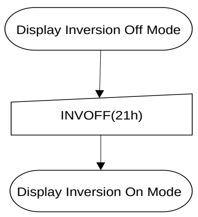
Display Inversion On Mode
INVOFF(20h)
Display Inversion Off Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

</td></tr>
</table>

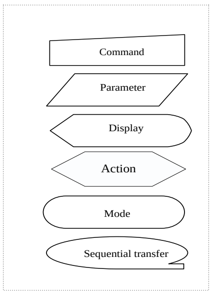
4.2.8. Display Inversion ON (21h)

<table>
<tr><th>21h</th><th colspan="13">Display Inversion ON</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into display inversion mode.
This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.
This command doesn’t change any other status.
To exit Display inversion mode, the Display inversion OFF command (20h) should be written..


memory
Display Panel

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion ON mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr>
<tr><td>SW Reset</td><td>Display Inversion OFF</td></tr>
<tr><td>HW Reset</td><td>Display Inversion OFF</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13">

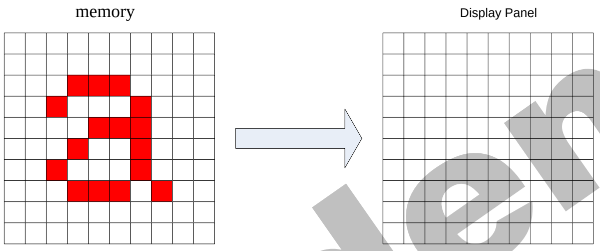
Display Inversion Off Mode
INVOFF(21h)
Display Inversion On Mode



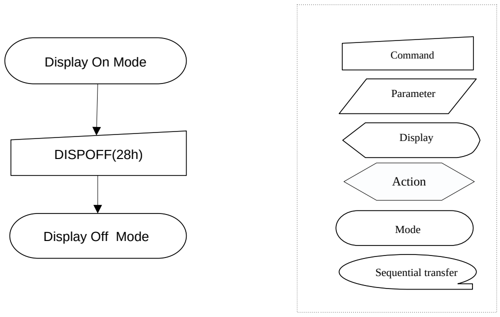
Command
Parameter
Display
Action
Mode
Sequential transfer

</td></tr>
</table>

4.2.9. Display OFF (28h)

<table>
<tr><td>28h</td><td colspan="13">Display OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.


memory
Display Panel

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">

Display On Mode
DISPOFF(28h)
Display Off Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

</td></tr>
</table>

4.2.10. Display ON (29h)

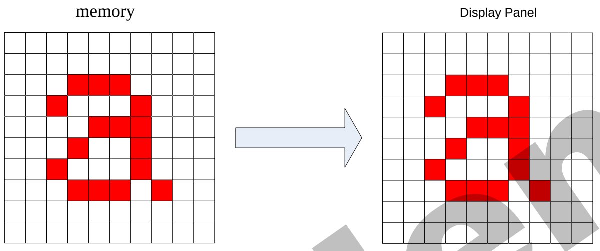
29h	Display ON											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter												

Description

This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.

This command makes no change of contents of frame memory.

This command does not change any other status.


memory
Display Panel

X = Don't care

Restriction

This command has no effect when module is already in display on mode.

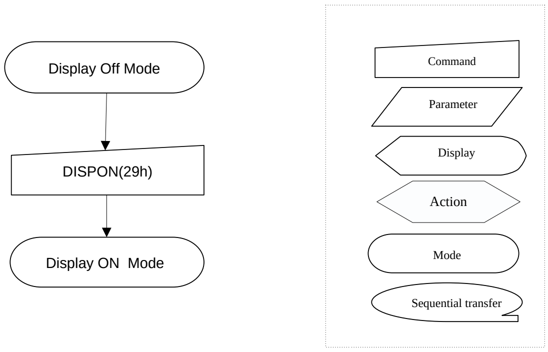
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

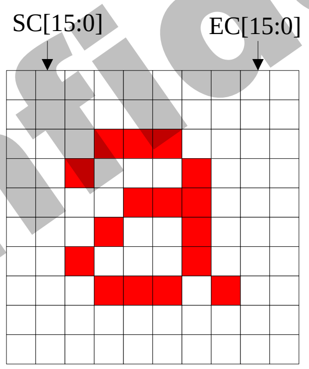

Display Off Mode
DISPON(29h)
Display ON Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

4.2.11. Column Address Set (2Ah)

2Ah	Column Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2nd Parameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory..



X = Don’t care

Restriction

SC [15:0] always must be equal to or less than EC [15:0].

Note 1: When SC [15:0] or EC [15:0] is greater than 009Fh (When MADCTL’s B5 = 0) or 009Fh (When MADCTL’s B5 = 1), data of out of range will be ignored

Register Availability

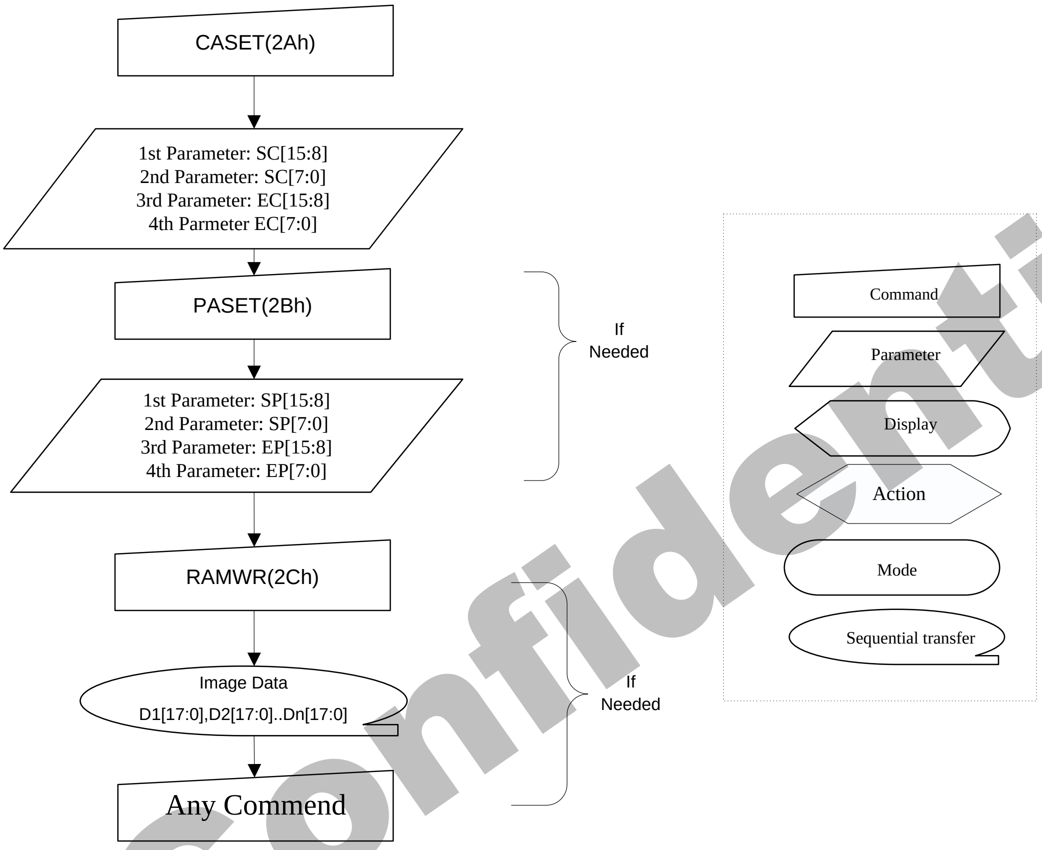
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

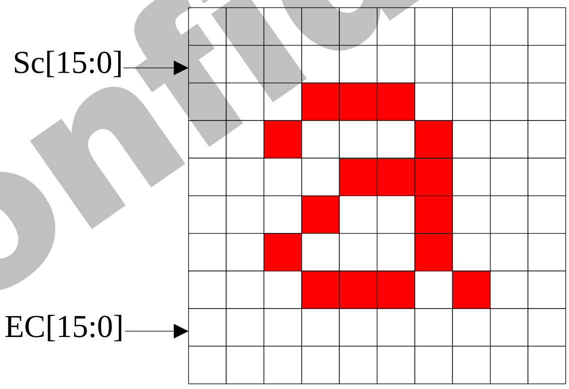
Status	Default Value	
Power On Sequence	SC [15:0]=0000h	EC [15:0]=009Fh

SW Reset	SC [15:0]=0000h	If MADCTL’s B5 = 0: EC [15:0]=009Fh
		If MADCTL’s B5 = 1: EC [15:0]=009Fh
HW Reset	SC [15:0]=0000h	EC [15:0]=009Fh

Flow Chart

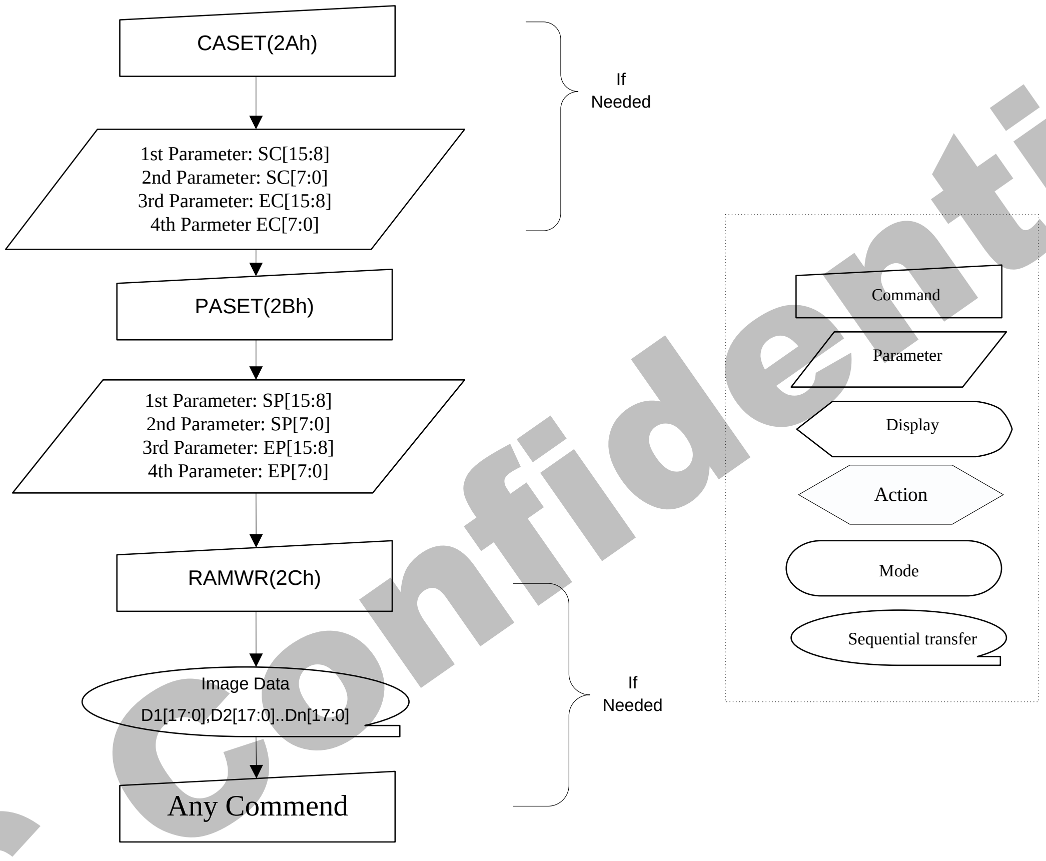

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
If Needed
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
If Needed
Command
Parameter
Display
Action
Mode
Sequential transfer

4.2.12. Row Address Set (2Bh)

<table>
<tr><td>2Bh</td><td colspan="13">Row Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP15</td><td>SP14</td><td>SP13</td><td>SP12</td><td>SP11</td><td>SP10</td><td>SP9</td><td>SP8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP7</td><td>SP6</td><td>SP5</td><td>SP4</td><td>SP3</td><td>SP2</td><td>SP1</td><td>SP0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP15</td><td>EP14</td><td>EP13</td><td>EP12</td><td>EP11</td><td>EP10</td><td>EP9</td><td>EP8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP7</td><td>EP6</td><td>EP5</td><td>EP4</td><td>EP3</td><td>EP2</td><td>EP1</td><td>EP0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.

X = Don't care</td></tr>
<tr><td>Restriction</td><td colspan="13">SP [15:0] always must be equal to or less than EP [15:0]
Note 1: When SP [15:0] or EP [15:0] is greater than 0009Fh (When MADCTL's B5 = 0) or 009Fh (When MADCTL's B5 = 1), data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

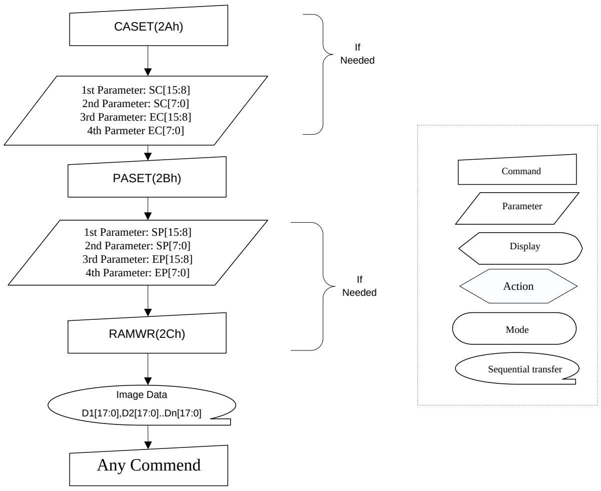
Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=00EFh
SW Reset	SP [15:0]=0000h	If MADCTL’s B5 = 0: EP [15:0]=009Fh
		If MADCTL’s B5 = 1: EP [15:0]=0009Fh
HW Reset	SP [15:0]=0000h	EP [15:0]=0009Fh

Flow Chart

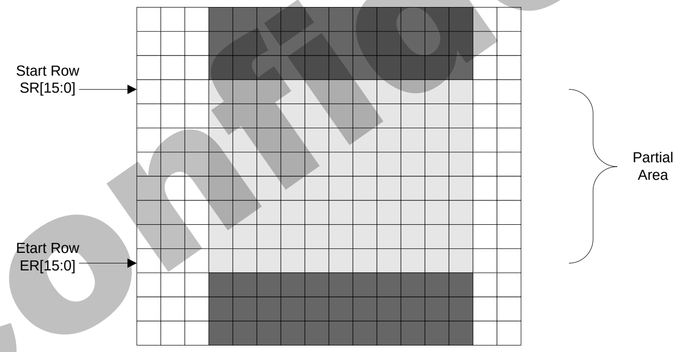
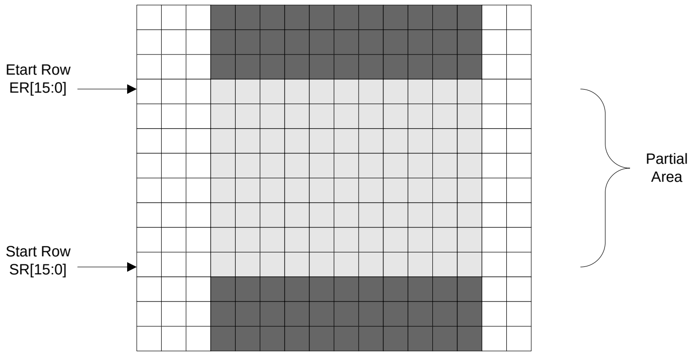

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
If Needed
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
If Needed
Command
Parameter
Display
Action
Mode
Sequential transfer

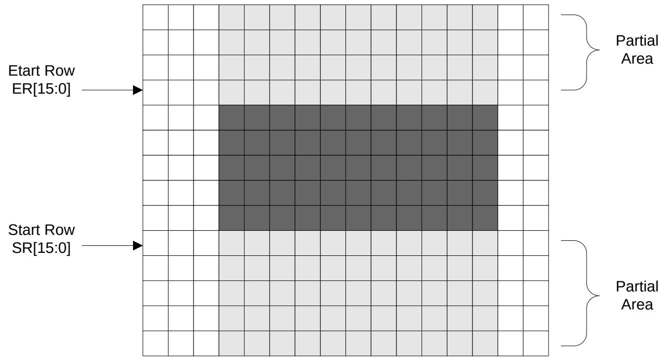
4.2.13. Memory Write (2Ch)

<table>
<tr><td>2Ch</td><td colspan="12">Memory Write</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2Ch</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">D1 [17:0]</td><td>XX</td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dx [17:0]</td><td>XX</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dn [17:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">In all color modes, there is no restriction on length of parameters.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr>
<tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr>
<tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr>
</table>
</td></tr>
</table>

Flow Chart	 CASET(2Ah) 1st Parameter: SC[15:8] 2nd Parameter: SC[7:0] 3rd Parameter: EC[15:8] 4th Parmeter EC[7:0] If Needed PASET(2Bh) 1st Parameter: SP[15:8] 2nd Parameter: SP[7:0] 3rd Parameter: EP[15:8] 4th Parameter: EP[7:0] If Needed RAMWR(2Ch) Image Data D1[17:0],D2[17:0]..Dn[17:0] Any Commend Command Parameter Display Action Mode Sequential transfer

4.2.14. Partial Area (30h)

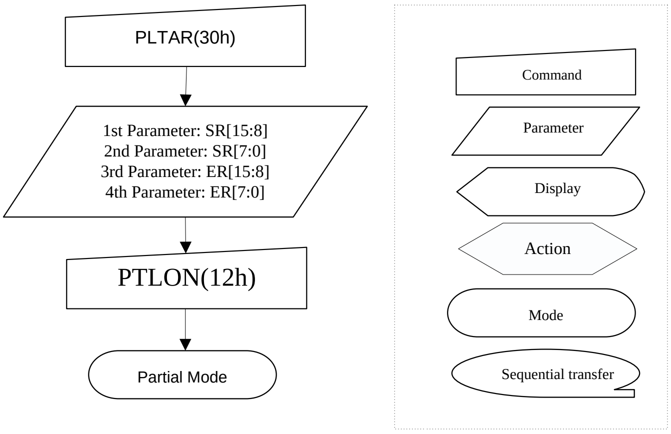
30h	Partial Area											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	67
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:-  Start Row SR[15:0] Etart Row ER[15:0] Partial Area If End Row>Start Row when MADCTL B4=1:-  Etart Row ER[15:0] Start Row SR[15:0] Partial Area If End Row<Start Row when MADCTL B4=0:-												

<table>
<tr><td></td><td>


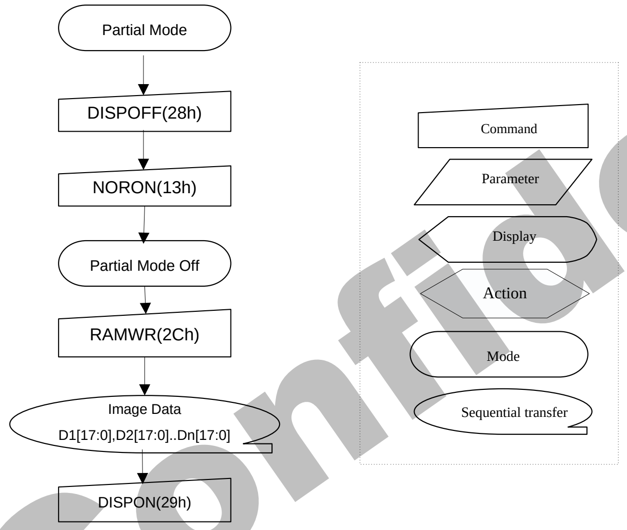
If End Row = Start Row then the Partial Area will be one row deep.
X = Don’t care.
</td></tr>
<tr><td>Restriction</td><td>SR [15…0] and ER [15…0] cannot be 0000h nor exceed 0167h.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>SR [15:0]</th><th>ER [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td><td>16’h0167h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td><td>16’h0167 h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td><td>16’h0167 h</td></tr>
</table>
</td></tr>
</table>

Flow Chart

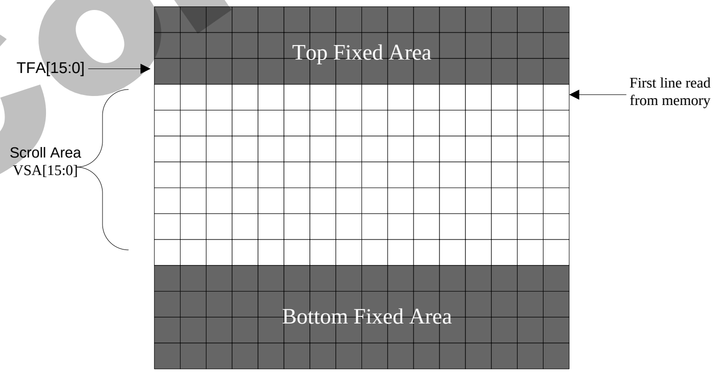
1. To Enter Partial Mode

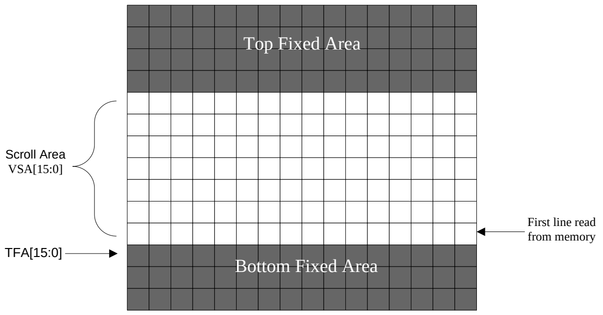

PLTAR(30h)
1st Parameter: SR[15:8]
2nd Parameter: SR[7:0]
3rd Parameter: ER[15:8]
4th Parameter: ER[7:0]
PTLON(12h)
Partial Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

2. To Leave Partial Mode


Partial Mode
DISPOFF(28h)
NORON(13h)
Partial Mode Off
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
DISPON(29h)
Command
Parameter
Display
Action
Mode
Sequential transfer

4.2.15. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								01
4th Parameter	1	1	↑	XX	VSA [7:0]								67
Description	This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.  TFA[15:0] Top Fixed Area First line read from memory Scroll Area VSA[15:0] Bottom Fixed Area When MADCTL B4=1 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.												


Top Fixed Area
Scroll Area
VSA[15:0]
TFA[15:0]
First line read
from memory
Bottom Fixed Area

X = Don’t care.

Restriction

Register Availability

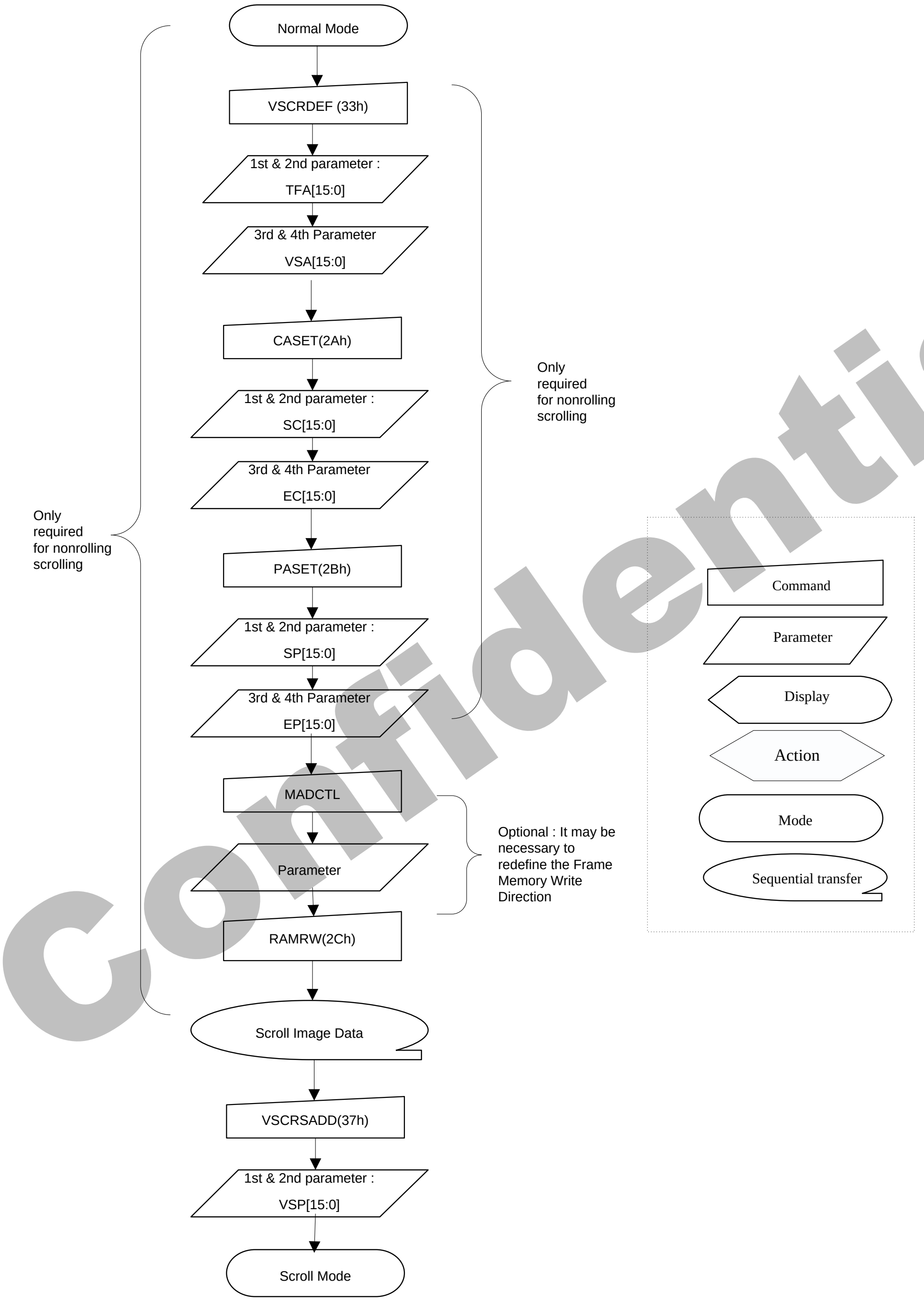
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16’h0000h	16’h0167h
SW Reset	16’h0000h	16’h0167h
HW Reset	16’h0000h	16’h0167h

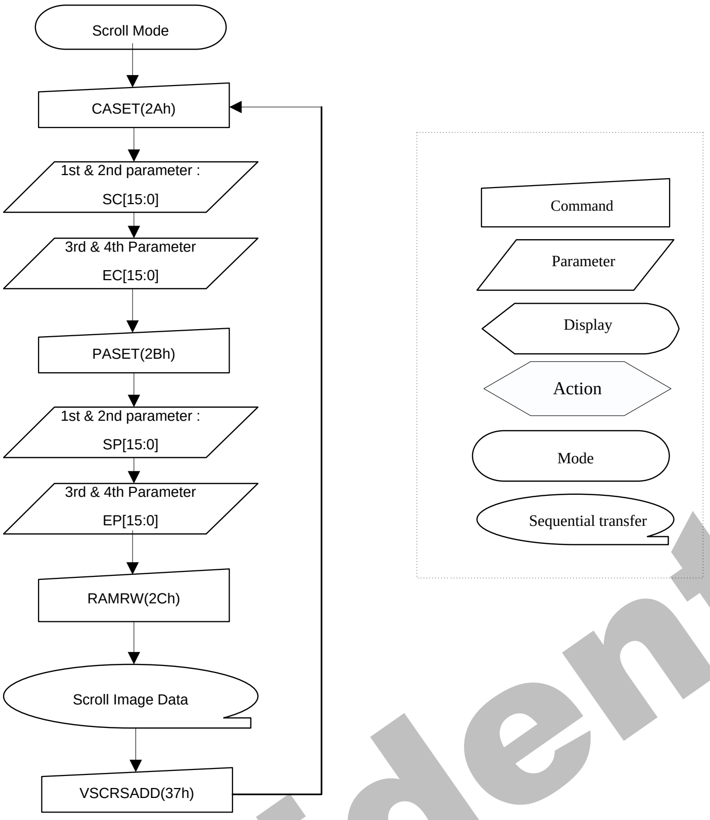
Flow Chart

1. To enter Vertical Scroll Mode :

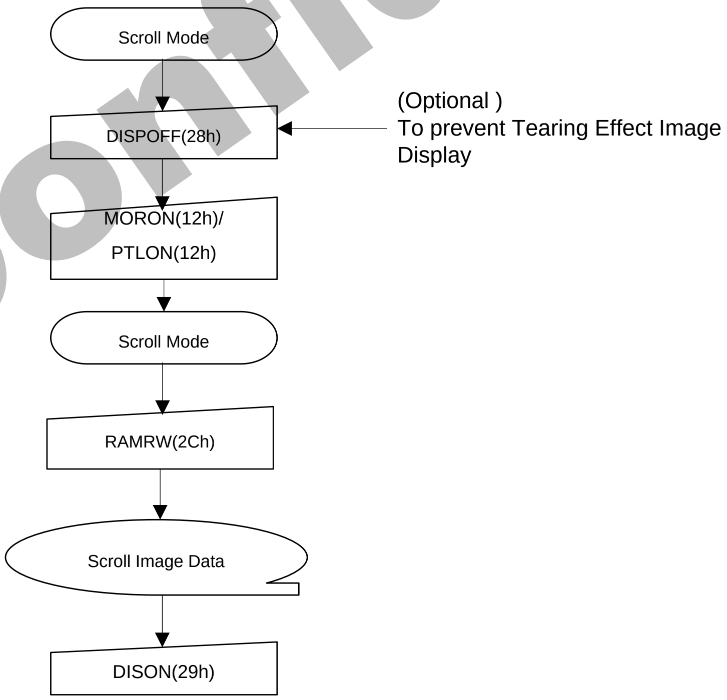

Normal Mode
VSCRDEF (33h)
1st & 2nd parameter :
TFA[15:0]
3rd & 4th Parameter
VSA[15:0]
CASET(2Ah)
1st & 2nd parameter :
SC[15:0]
3rd & 4th Parameter
EC[15:0]
PASET(2Bh)
1st & 2nd parameter :
SP[15:0]
3rd & 4th Parameter
EP[15:0]
MADCTL
Parameter
RAMRW(2Ch)
Scroll Image Data
VSCRSADD(37h)
1st & 2nd parameter :
VSP[15:0]
Scroll Mode
Only required for nonrolling scrolling
Only required for nonrolling scrolling
Optional : It may be necessary to redefine the Frame Memory Write Direction
Command
Parameter
Display
Action
Mode
Sequential transfer

Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :

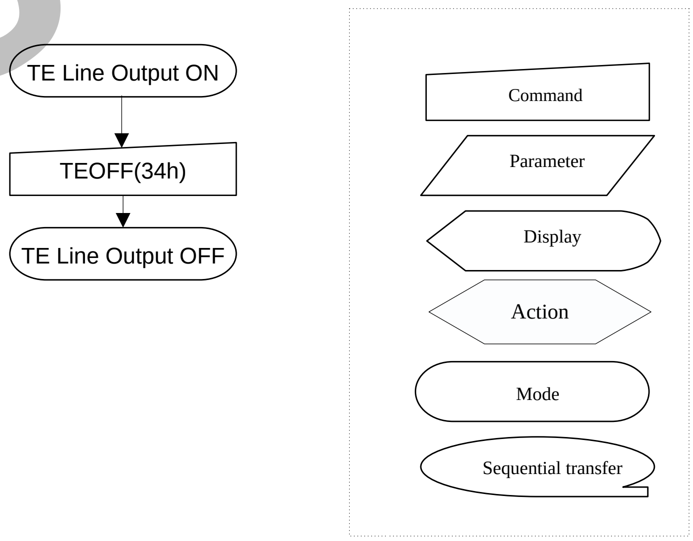

Scroll Mode
CASET(2Ah)
1st & 2nd parameter :
SC[15:0]
3rd & 4th Parameter
EC[15:0]
PASET(2Bh)
1st & 2nd parameter :
SP[15:0]
3rd & 4th Parameter
EP[15:0]
RAMRW(2Ch)
Scroll Image Data
VSCRSADD(37h)
Command
Parameter
Display
Action
Mode
Sequential transfer

3.To Leave Vertical Scroll Mode:


Scroll Mode
DISPOFF(28h)
(Optional)
To prevent Tearing Effect Image
Display
MORON(12h)/
PTLON(12h)
Scroll Mode
RAMRW(2Ch)
Scroll Image Data
DISON(29h)

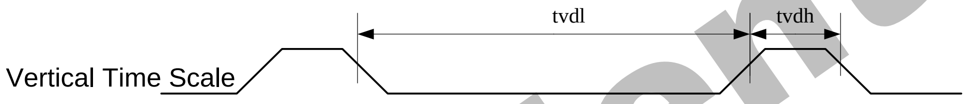
Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

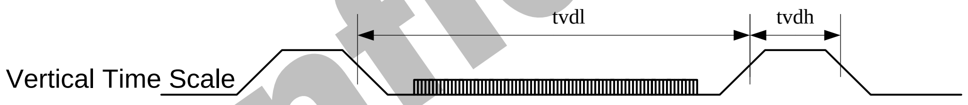
4.2.16. Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>OFF</td></tr>
<tr><td>SW Reset</td><td>OFF</td></tr>
<tr><td>HW Reset</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13">

TE Line Output ON
TEOFF(34h)
TE Line Output OFF
Command
Parameter
Display
Action
Mode
Sequential transfer
</td></tr>
</table>

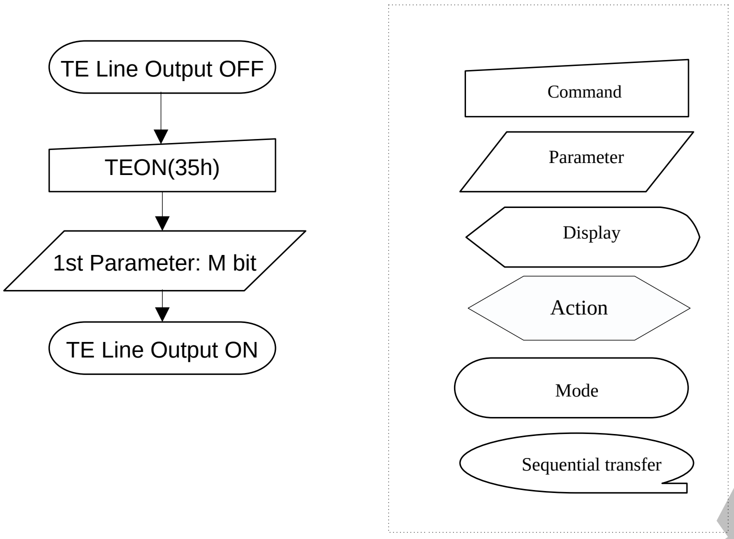
4.2.17. Tearing Effect Line ON (35h)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">
This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:
The Tearing Effect Output line consists of V-Blanking information only:


When **M=1**:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:


Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don't care.
</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>OFF</td></tr>
<tr><td>SW Reset</td><td>OFF</td></tr>
<tr><td>HW Reset</td><td>OFF</td></tr>
</table>
</td></tr>
</table>

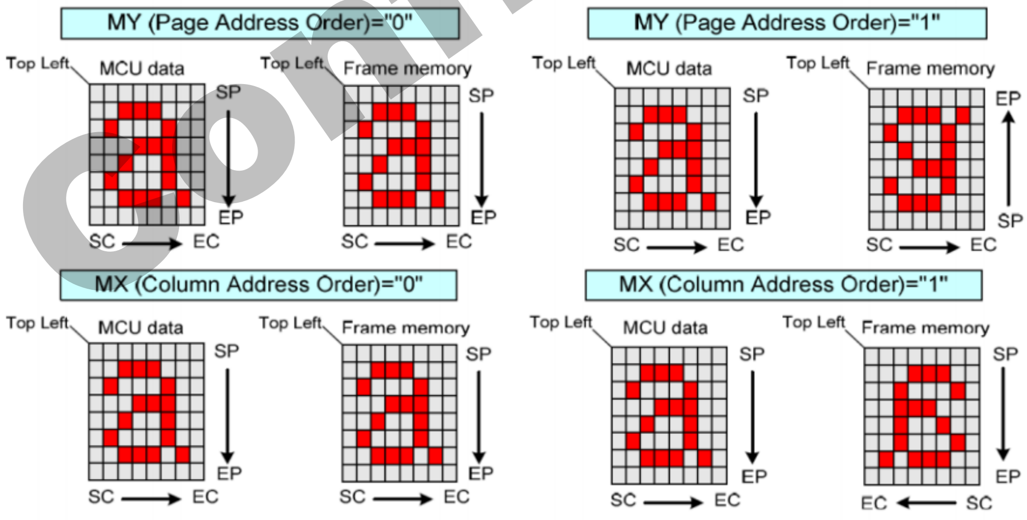
Flow Chart	TE Line Output OFF TEON(35h) 1st Parameter: M bit TE Line Output ON Command Parameter Display Action Mode Sequential transfer

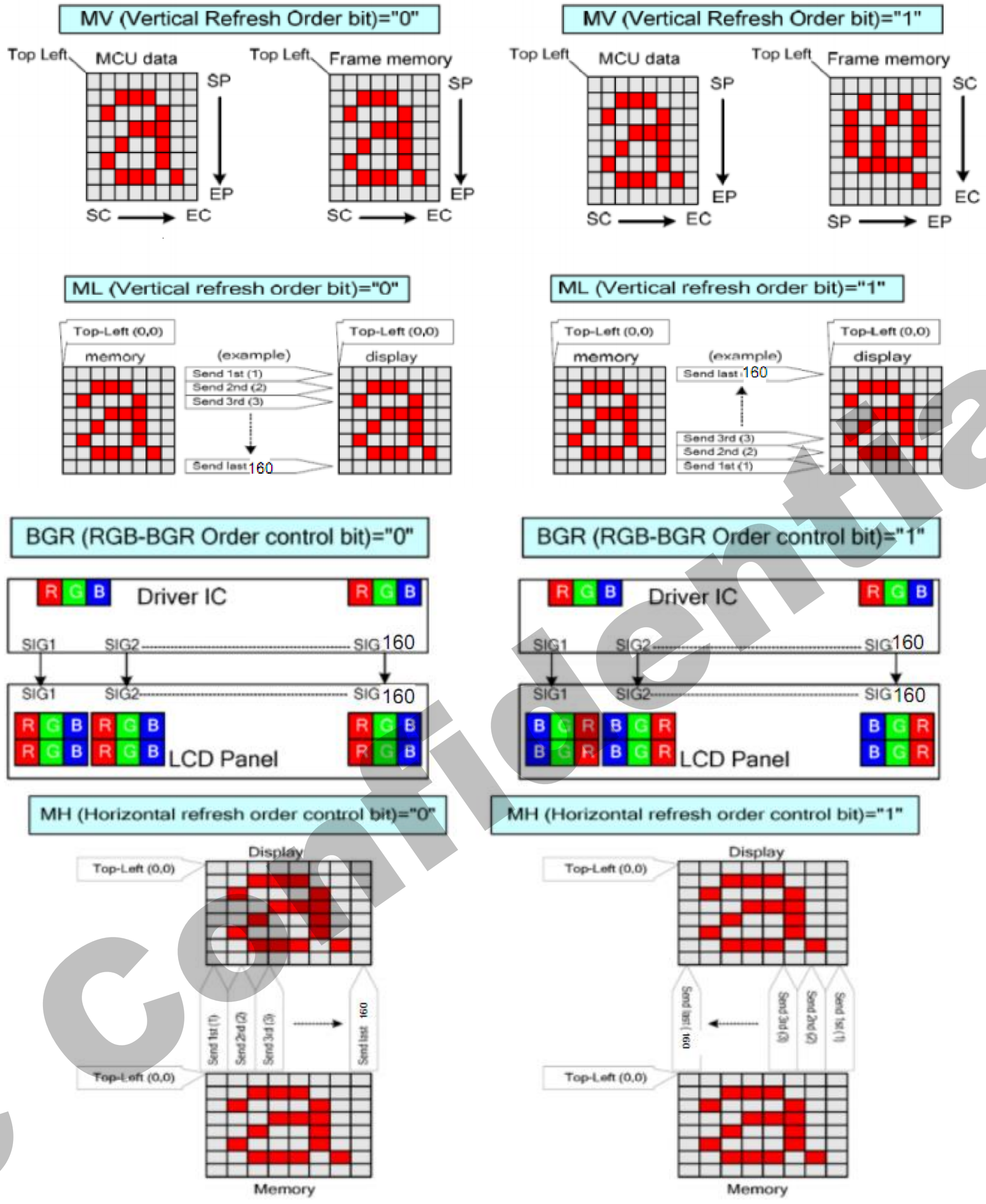
4.2.18. Memory Access Control(36h)

36h	Tearing Effect Line ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00
Description	This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.												

Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

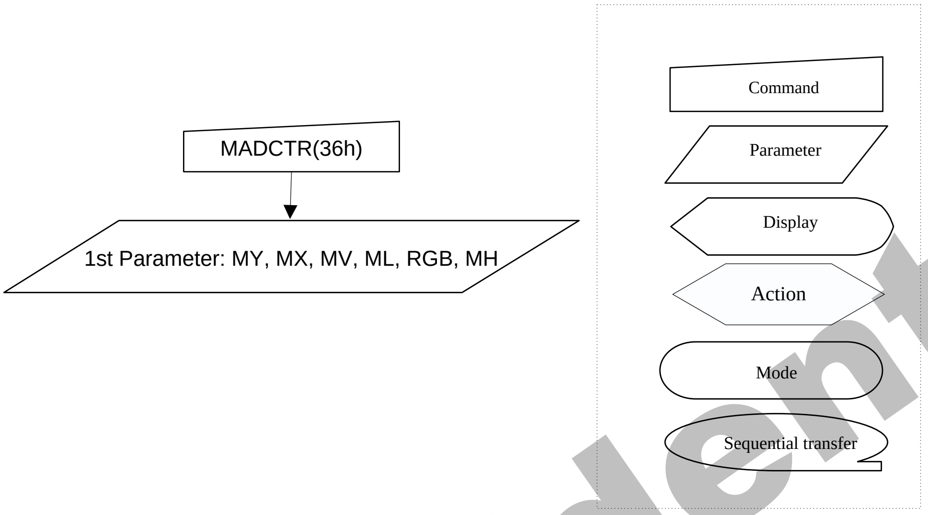
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.


MY (Page Address Order)="0"
MY (Page Address Order)="1"
Top Left
MCU data
Frame memory
SP
EP
SC
EC
MX (Column Address Order)="0"
MX (Column Address Order)="1"

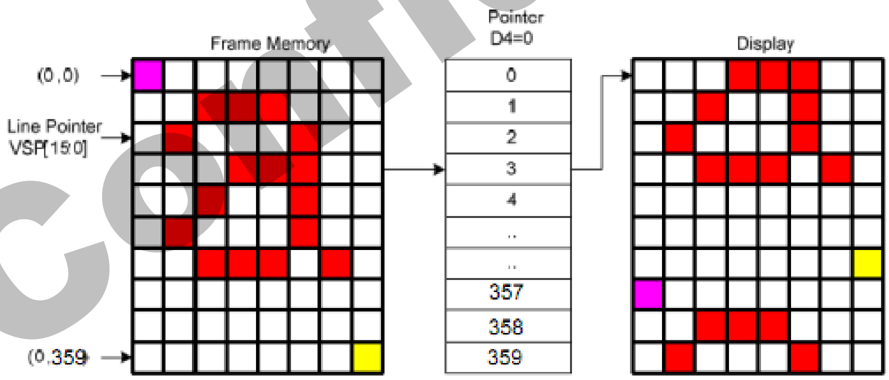
<table>
<tr><td></td><td>

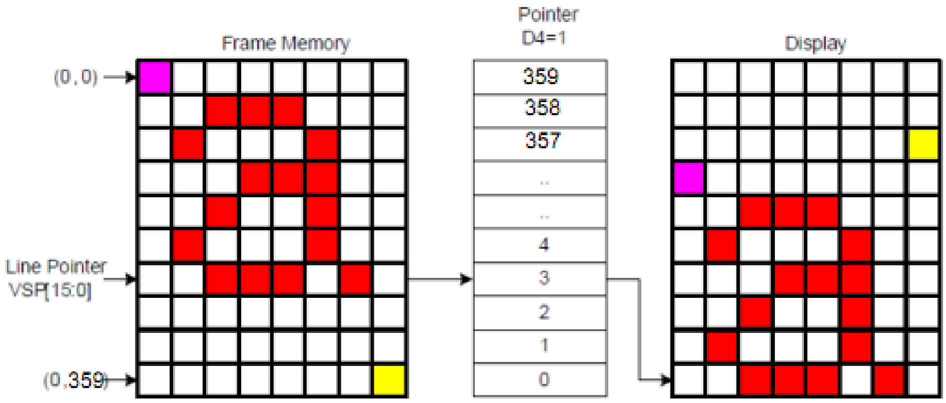
MV (Vertical Refresh Order bit)="0"
Top Left
MCU data
SP
EP
SC
EC
Top Left
Frame memory
SP
EP
SC
EC
MV (Vertical Refresh Order bit)="1"
Top Left
MCU data
SP
EP
SC
EC
Top Left
Frame memory
SC
EC
SP
EP
ML (Vertical refresh order bit)="0"
Top-Left (0,0)
memory
(example)
Send 1st (1)
Send 2nd (2)
Send 3rd (3)
Send last 160
Top-Left (0,0)
display
ML (Vertical refresh order bit)="1"
Top-Left (0,0)
memory
(example)
Send last 160
Send 3rd (3)
Send 2nd (2)
Send 1st (1)
Top-Left (0,0)
display
BGR (RGB-BGR Order control bit)="0"
R G B
Driver IC
R G B
SIG1
SIG2
SIG160
SIG1
SIG2
SIG160
R G B R G B
R G B R G B
LCD Panel
R G B
R G B
BGR (RGB-BGR Order control bit)="1"
R G B
Driver IC
R G B
SIG1
SIG2
SIG160
SIG1
SIG2
SIG160
B G R B G R
B G R B G R
LCD Panel
B G R
B G R
MH (Horizontal refresh order control bit)="0"
Display
Top-Left (0,0)
Send 1st (1)
Send 2nd (2)
Send 3rd (3)
Send last 160
Top-Left (0,0)
Memory
MH (Horizontal refresh order control bit)="1"
Display
Top-Left (0,0)
Send last 160
Send 3rd (3)
Send 2nd (2)
Send 1st (1)
Top-Left (0,0)
Memory

Note: Top-Left (0,0) means a physical memory location.</td></tr>
<tr><td>Restriction</td><td>This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>

MADCTR(36h)
1st Parameter: MY, MX, MV, ML, RGB, MH
Command
Parameter
Display
Action
Mode
Sequential transfer
</td></tr>
</table>

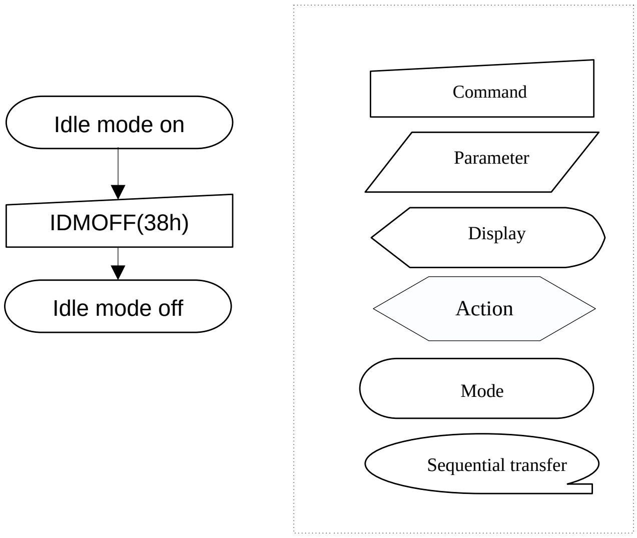
4.2.19. Vertical Scrolling Start Address (37h)

37h	**VSCRSADD (Vertical Scrolling Start Address)**											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	XX	VSP [15:8]								00
2nd Parameter	1	1	↑	XX	VSP [7:0]								00
Description	This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:- When MADCTL B4=0 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 160 and VSP='3'.  Frame Memory (0,0) Line Pointer VSP[15:0] (0,359) Pointer D4=0 0 1 2 3 4 .. .. 357 358 359 Display When MADCTL B4=1 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 160 and VSP='3'.												

	 Frame Memory Pointer D4=1 Display (0,0) Line Pointer VSP[15:0] (0,359) 359 358 357 .. .. 4 3 2 1 0 *Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.* *(2) This command is ignored when the GC9D01N enters Partial mode.* X = Don’t care
Restriction	This command has no effect when Tearing Effect output is already ON

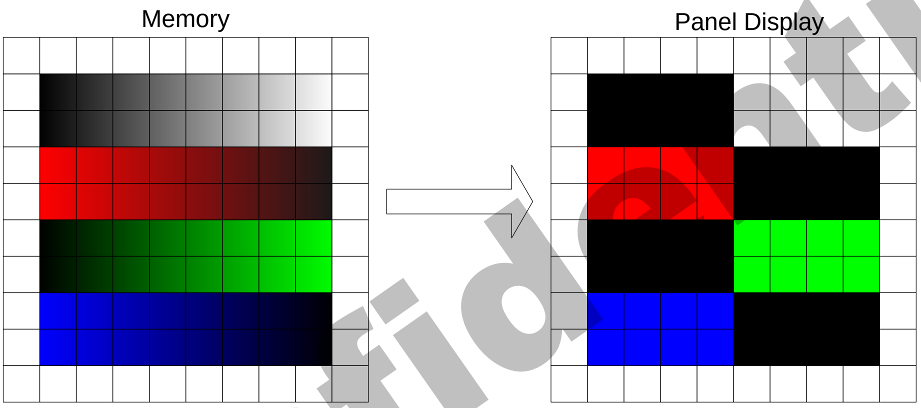
<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

4.2.20. Idle Mode OFF (38h)

<table>
<tr><th>38h</th><th colspan="13">Idle Mode OFF</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr>
<tr><td>SW Reset</td><td>Idle mode OFF</td></tr>
<tr><td>HW Reset</td><td>Idle mode OFF</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13">
Idle mode on
IDMOFF(38h)
Idle mode off
Command
Parameter
Display
Action
Mode
Sequential transfer

</td></tr>
</table>

4.2.21. Idle Mode ON (39h)

<table>
<tr><td>39h</td><td colspan="13">Idle Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.


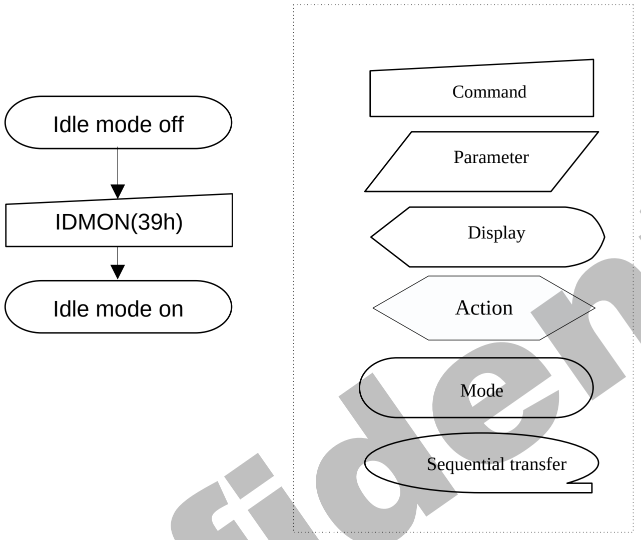
<table>
<tr><td></td><td colspan="3">Memory Contents vs. Display Color</td></tr>
<tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr>
<tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr>
<tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr>
</table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
</table>

Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>

<table>
<tr>
<td>Default</td>
<td>

<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr>
<tr><td>SW Reset</td><td>Idle mode OFF</td></tr>
<tr><td>HW Reset</td><td>Idle mode OFF</td></tr>
</table>

</td>
</tr>
<tr>
<td>Flow Chart</td>
<td>


Idle mode off
IDMON(39h)
Idle mode on
Command
Parameter
Display
Action
Mode
Sequential transfer

</td>
</tr>
</table>

4.2.22. COLMOD: Pixel Format Set (3Ah)

3Ah	Pixel Format Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
Parameter	1	1	↑	XX	0	DPI [2:0]			0	DBI [2:0]			66

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	12 bits / pixel
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

If using RGB Interface must selection serial interface.

X = Don't care.

Restriction

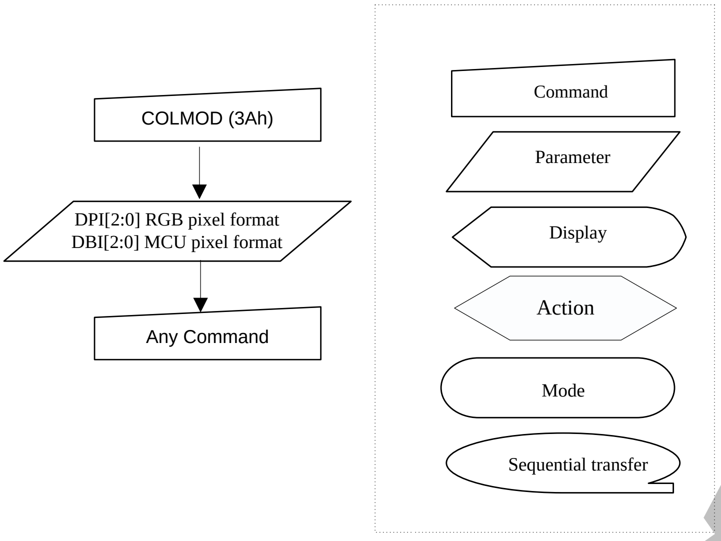
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

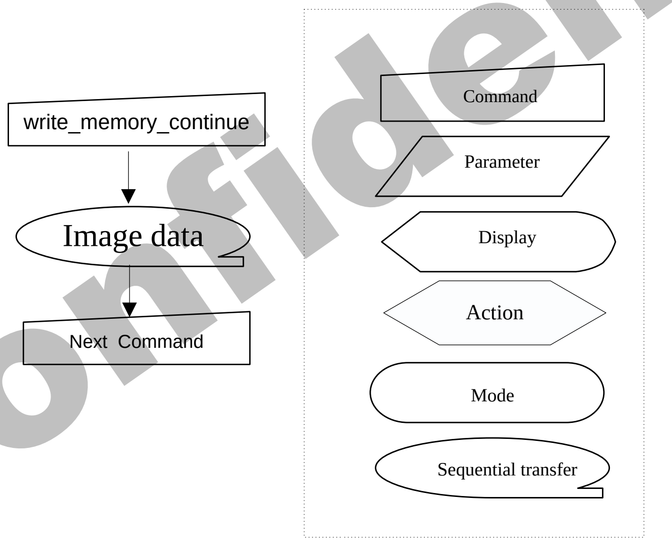
Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b110	3'b110
SW Reset	No Change	No Change
HW Reset	3'b110	3'b110

Flow Chart	COLMOD (3Ah) DPI[2:0] RGB pixel format DBI[2:0] MCU pixel format Any Command Command Parameter Display Action Mode Sequential transfer

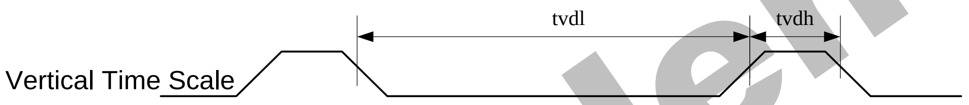
4.2.23. Write Memory Contiue (3Ch)

3Ch	write_memory_continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	D1[17..8]	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	Dx[17..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	0003FF
Xth Parameter	1	1	↑	D1[17..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	0003FF
Nth Parameter	1	1	↑	Dn[17..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	0003FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC –SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP –SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.												

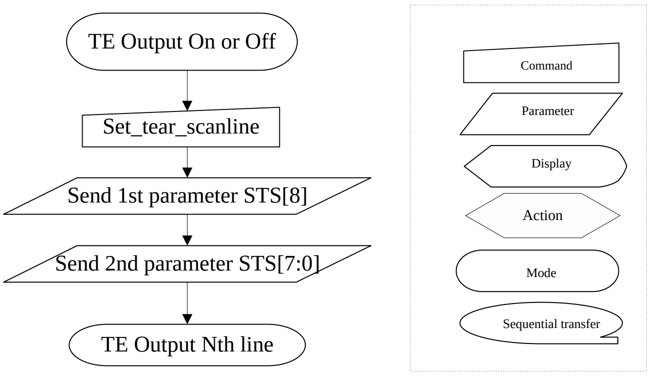
	Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Random value</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>No change</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>

write_memory_continue
Image data
Next Command
Command
Parameter
Display
Action
Mode
Sequential transfer
</td></tr>
</table>

4.2.24. Set_Tear_Scanline (44h)

<table>
<tr><td>44h</td><td colspan="13">Set_Tear_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>STS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>STS [7]</td><td>STS [6]</td><td>STS [5]</td><td>STS [4]</td><td>STS [3]</td><td>STS [2]</td><td>STS [1]</td><td>STS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of STS[8:0]


Note:that set_tear_scanline with STS is equivalent to set_tear_on with 8+GateN(N=1、2、3...260)
eg:when the STS[8:0]=8,the TE will output at the position of Gate1.
when the STS[8:0]=9,the TE will output at the position of Gate2.
when the STS[8:0]=10,the TE will output at the position of Gate3.
……….
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>STS [8:0]=0000h</td></tr>
<tr><td>SW Reset</td><td>STS [8:0]=0000h</td></tr>
<tr><td>HW Reset</td><td>STS [8:0]=0000h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	TE Output On or Off Set_tear_scanline Send 1st parameter STS[8] Send 2nd parameter STS[7:0] TE Output Nth line Command Parameter Display Action Mode Sequential transfer

4.2.25. Get_Scanline (45h)

45h	Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	0	0	0	0	0	0	0	GTS [8]	00
2nd Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00
Description	This command returns the setting value of STS[8:0] . When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	None												

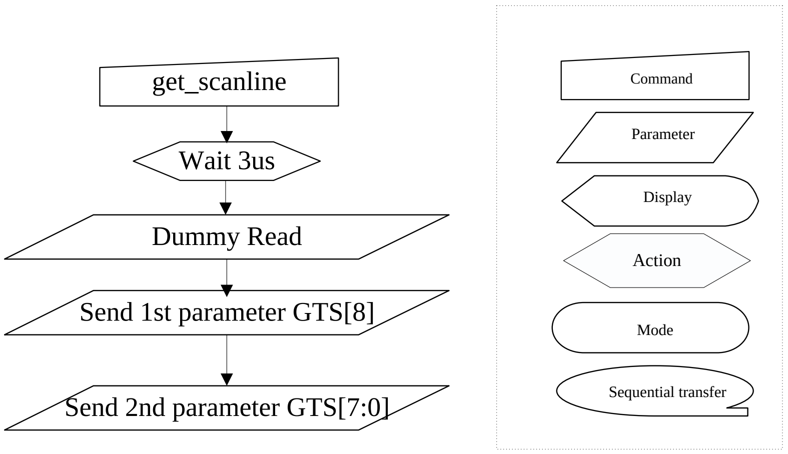
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

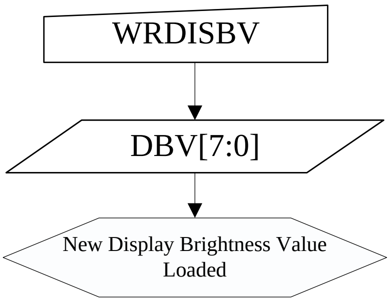
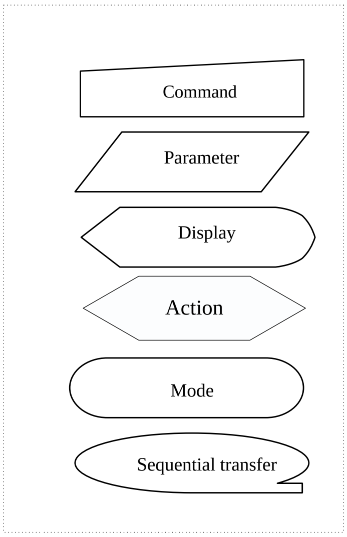
Default

Status	Default Value
Power On Sequence	GTS [9:0]=0000h
SW Reset	GTS [9:0]=0000h
HW Reset	GTS [9:0]=0000h

Flow Chart


get_scanline
Wait 3us
Dummy Read
Send 1st parameter GTS[8]
Send 2nd parameter GTS[7:0]
Command
Parameter
Display
Action
Mode
Sequential transfer

4.2.26. Write Display Brightness (51h)

<table>
<tr><th>51h</th><th colspan="13">Write Display Brightness</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>51h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>DBV[7]</td><td>DBV[6]</td><td>DBV[5]</td><td>DBV[4]</td><td>DBV[3]</td><td>DBV[6]</td><td>DBV[5]</td><td>DBV[4]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to adjust the brightness value of the display.
It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>DBV [7:0]= 8’h00</td></tr>
<tr><td>SW Reset</td><td>DBV [7:0]= 8’h00</td></tr>
<tr><td>HW Reset</td><td>DBV [7:0]= 8’h00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13">

WRDISBV
DBV[7:0]
New Display Brightness Value Loaded

Command
Parameter
Display
Action
Mode
Sequential transfer
</td></tr>
</table>

4.2.27. Write CTRL Display (53h)

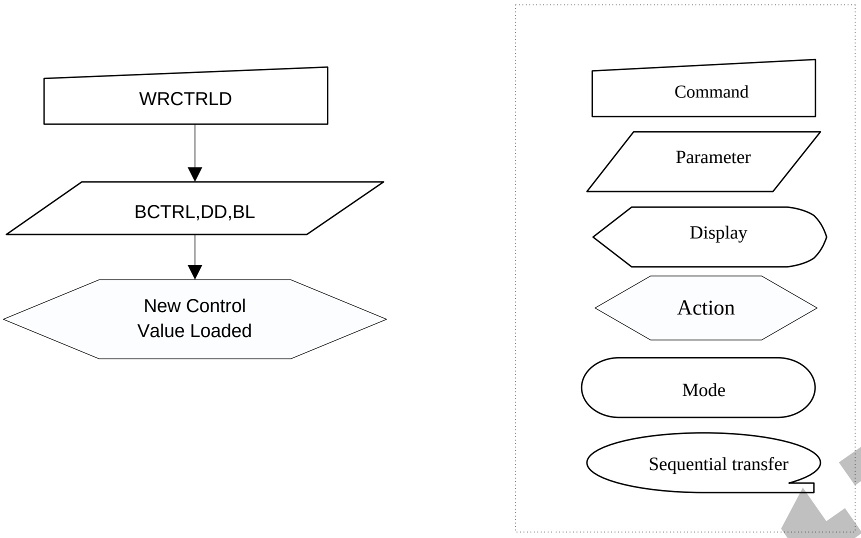
53h	Write CTRL Display												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
1st Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00
Description	This command is used to return brightness setting. **BCTRL**: Brightness Control Block On/Off, ‘0’ = Off (Brightness registers are 00h) ‘1’ = On (Brightness registers are active, according to the DBV[7..0] parameters.) **DD**: Display Dimming ‘0’ = Display Dimming is off ‘1’ = Display Dimming is on **BL**: Backlight On/Off ‘0’ = Off (Completely turn off backlight circuit. Control lines must be low.) ‘1’ = On												
Restriction	The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

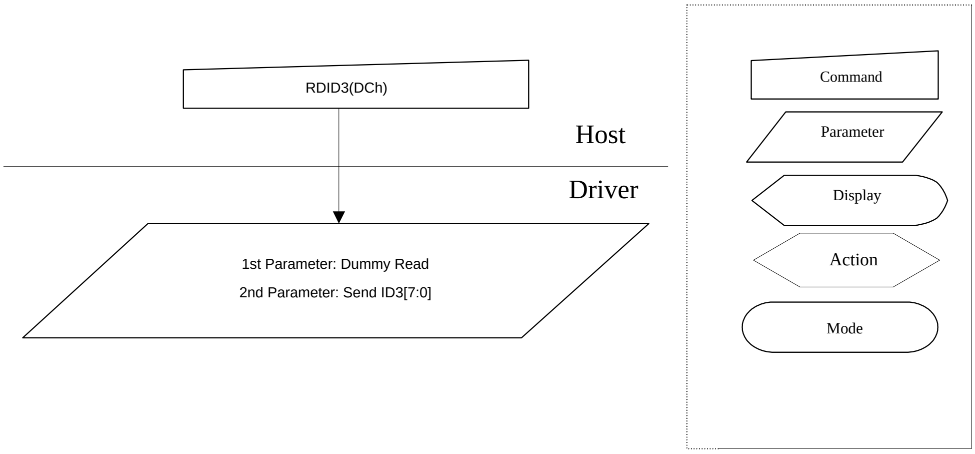
Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1’b0	1’b0	1’b0
SW Reset	1’b0	1’b0	1’b0
HW Reset	1’b0	1’b0	1’b0

Flow Chart	WRCTRLD BCTRL,DD,BL New Control Value Loaded Command Parameter Display Action Mode Sequential transfer

4.2.28. Read ID1 (DAh)

<table>
<tr><th>DCh</th><th colspan="13">Read ID2</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>DAh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3 [7:0]</td><td>Program value</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value
(After MTP program)</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>SW Reset</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

RDID3(DCh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send ID3[7:0]
Command
Parameter
Display
Action
Mode

4.2.29. Read ID2 (DBh)

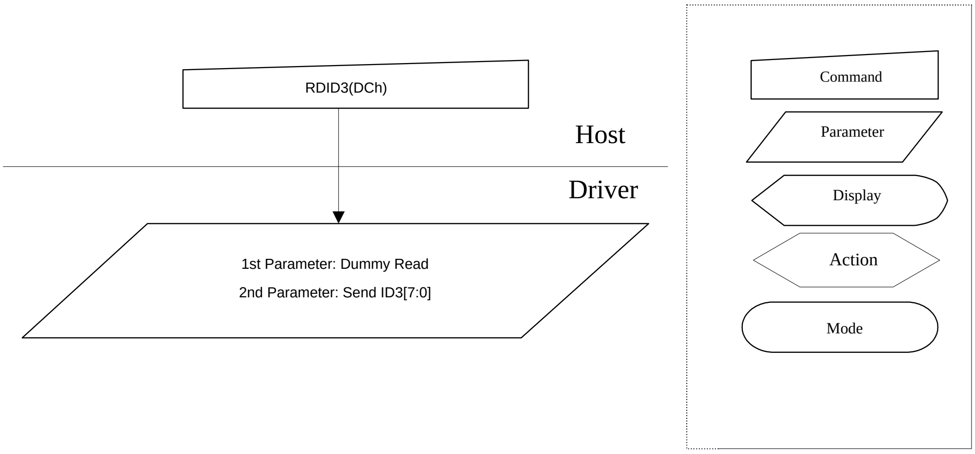
DCh	Read ID2											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								Program value
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

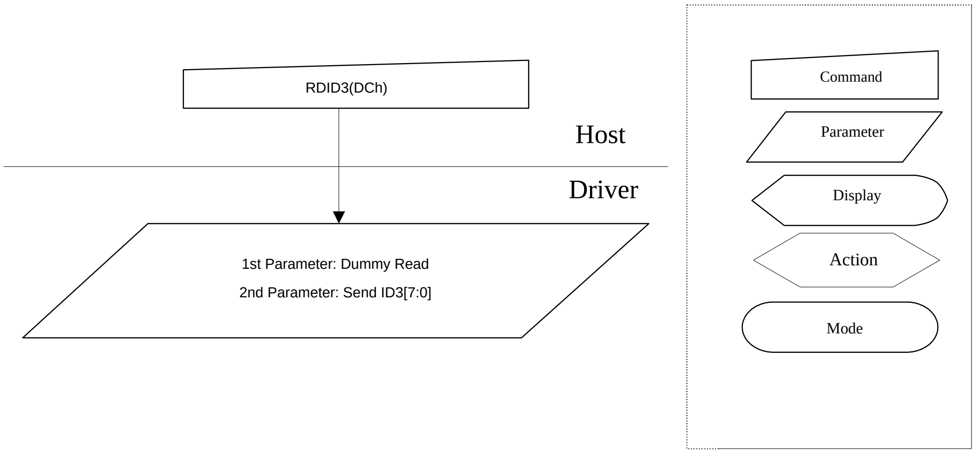
Default

Status	Default Value (After MTP program)
Power On Sequence	8'h9C
SW Reset	8'h9C
HW Reset	8'h9C

Flow Chart	RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

4.2.30. Read ID3 (DCh)

<table>
<tr><td>DCh</td><td colspan="13">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>DCh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3 [7:0]</td><td>Program value</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value (After MTP program)</th></tr>
<tr><td>Power On Sequence</td><td>8’h01</td></tr>
<tr><td>SW Reset</td><td>8’h01</td></tr>
<tr><td>HW Reset</td><td>8’h01</td></tr>
</table>
</td></tr>
</table>

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

4.3. Description of Level 2 Command

4.3.1. RGB Interface Signal Control (B0h)

<table>
<tr><td>B0h</td><td colspan="13">RGB Interface Signal Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="2">RCM[1：0]</td><td>0</td><td>VSPL</td><td>HSPL</td><td>DPL</td><td>EPL</td><td>01</td></tr>
<tr><td>Description</td><td colspan="13">
Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.
EPL: DE polarity (“0”= High enable for RGB interface, “1”= Low enable for RGB interface)
DPL: DOTCLK polarity set (“0”= data fetched at the rising time, “1”= data fetched at the falling time)
HSPL: HSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
RCM [1:0]: RGB interface selection (refer to the RGB interface section).
<table>
<tr><td colspan="2">RCM [1:0]</td><td>RIM</td><td colspan="3">DPI[1:0]</td><td>RGB interface Mode</td><td>RGB Mode</td><td>Used Pins</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB interface (262K colors)</td><td rowspan="3">DE Mode
Valid data is determined by the DE signal</td><td>VSYNC,HSYNC,DE, DOTCLK,D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB interface (65K colors)</td><td>VSYNC,HSYNC,DE, DOTCLK,D[17:13] & D[11:1]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td colspan="3">-</td><td>6-bit RGB interface (262K colors)</td><td>VSYNC,HSYNC,DE, DOTCLK,D[5:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB interface (262K colors)</td><td rowspan="3">SYNC Mode
In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command</td><td>VSYNC,HSYNC,DOTCLK, D[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB interface (65K colors)</td><td>VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="3">-</td><td>6-bit RGB interface (262K colors)</td><td>VSYNC,HSYNC,DOTCLK, D[5:0]</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
</table>

	Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

	Status	Default Value				
		RCM[1:0]	VSPL	HSPL	DPL	EPL
Default	Power On Sequence	2’b00	1’b0	1’b0	1’b0	1’b1
	SW Reset	2’b00	1’b0	1’b0	1’b0	1’b1
	HW Reset	2’b00	1’b0	1’b0	1’b0	1’b1

HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31

11111	32
HBP [4:0]	Number of HSYNC of front/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32
HBP [4:0]	Number of HSYNC of front/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32

4.3.2. Blanking Porch Control (B5h)

B5h	Blanking Porch Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	VFP [7:0]								08
2nd Parameter	1	1	↑	XX	0	VBP [6:0]							08
3rd Parameter	1	1	↑	XX	0	0	0	HBP [4:0]					14

Description

Note: The Third parameter must write,but it is not valid.

VFP [6:0] / VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	109.5
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HBP [4:0]: HBP [4:0] bits specify the line number of horizontal back porch period respectively.

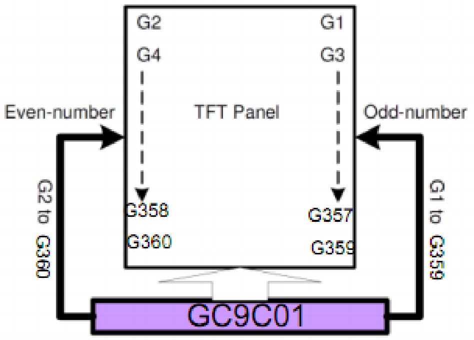
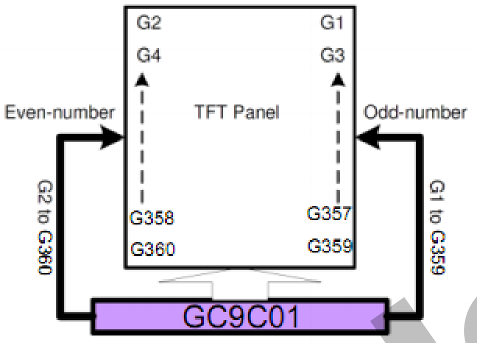
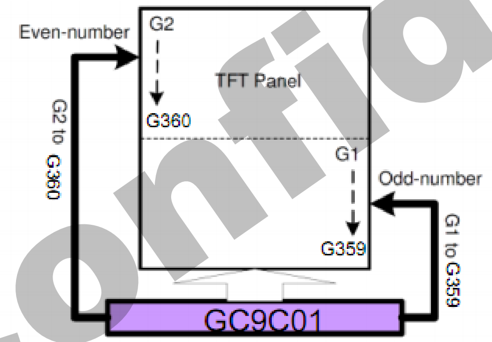
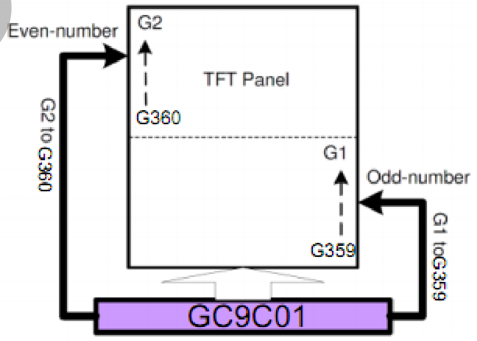
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HBP [4:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h08</td><td>7’h08</td><td>5’h14</td></tr>
<tr><td>SW Reset</td><td>7’h08</td><td>7’h08</td><td>5’h14</td></tr>
<tr><td>HW Reset</td><td>7’h08</td><td>7’h08</td><td>5’h14</td></tr>
</table>
</td></tr>
</table>

4.3.3. Display Function Control (B6h)

<table>
<tr><th>B6h</th><th colspan="13">Display Function Control</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>B6h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>GS</td><td>SS</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">
note:the first parameter must write,but it is not valid.
SS: Select the shift direction of outputs from the source driver.
<table>
<tr><th>SS</th><th>Source Output Scan Direction</th></tr>
<tr><td>0</td><td>S1 → S240</td></tr>
<tr><td>1</td><td>S240 → S1</td></tr>
</table>
In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.
To assign R, G, B dots to the source driver pins from S1 to S360, set SS = 0.
To assign R, G, B dots to the source driver pins from S360 to S1, set SS = 1.

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.
<table>
<tr><th>GS</th><th>Gate Output Scan Direction</th></tr>
<tr><td>0</td><td>G1→G160</td></tr>
<tr><td>1</td><td>G160→G1</td></tr>
</table>
</td></tr>
</table>

SM	GS	Scan Direction	Gate Output Sequence
0	0	 G2 G4 G1 G3 Even-number TFT Panel Odd-number G358 G360 G357 G359 G2 to G360 G1 to G359 GC9C01	G1→G2→G3→G4→ ....→G357→G358→G359→G360
0	1	 G2 G4 G1 G3 Even-number TFT Panel Odd-number G358 G360 G357 G359 G2 to G360 G1 to G359 GC9C01	G360 →G359→G358→G357→...... .... →G4→G3→G2→G1
1	0	 Even-number G2 TFT Panel G360 G1 Odd-number G359 G2 to G360 G1 to G359 GC9C01	G1→G3→...........→G357→G359→ G2→G4→...........→G358→G360
1	1	 Even-number G2 TFT Panel G360 G1 Odd-number G359 G2 to G360 G1 toG359 GC9C01	G360→G358→...........→G4→G2→ G359→G357→...........→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL [5:0]	LCD Drive Line	NL [5:0]	LCD Drive Line

0	0	0	0	0	0	Setting prohibited	0	1	0	1	0	1	176 lines
0	0	0	0	0	1	16 lines	0	1	0	1	1	0	184 lines
0	0	0	0	1	0	24 lines	0	1	0	1	1	1	192 lines
0	0	0	0	1	1	32 lines	0	1	1	0	0	0	200 lines
0	0	0	1	0	0	40 lines	0	1	1	0	0	1	208 lines
0	0	0	1	0	1	48 lines	……						
0	0	0	1	1	0	56 lines	1	1	0	0	1	1	344 lines
0	0	0	1	1	1	64 lines	1	1	0	1	0	0	352 lines
0	0	1	0	0	0	72 lines	1	1	0	1	0	1	360 lines
0	0	1	0	0	1	80 lines	Others						Setting prohibited
0	0	1	0	1	0	88 lines							
0	0	1	0	1	1	96 lines							
0	0	1	1	0	0	104 lines							
0	0	1	1	0	1	112 lines							
0	0	1	1	1	0	120 lines							
0	0	1	1	1	1	128 lines							
0	1	0	0	0	0	136 lines							
0	1	0	0	0	1	144 lines							
0	1	0	0	1	0	152 lines							
0	1	0	0	1	1	160 lines							

Restriction	EXTC should be high to enable this command

Register Availability

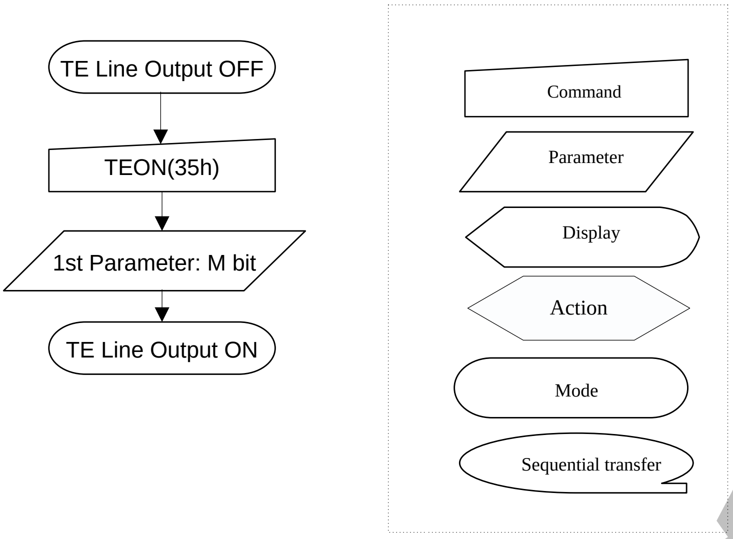
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	-	GS	SS	/
Power On Sequence	-	1’b0	1’b0	/
HW Resset	-	1’b0	1’b0	/

4.3.4. Tearing Effect Control (B4h)

<table>
<tr><th>B4h</th><th colspan="13">Tearing Effect Width Control</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>B4h</td></tr>
<tr><td>Parameter1</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">te_width[7:0]</td><td>00</td></tr>
<tr><td>Parameter2</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>te_pol</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">te_pol is used to adjust the Tearing Effect output signal pulse polarity.
<table>
<tr><th>te_pol</th><th>Tearing Effect polarity</th></tr>
<tr><td>0</td><td>Positive pulse</td></tr>
<tr><td>1</td><td>negative pulse</td></tr>
</table>
te_width[6:0] is used to adjust the Tearing Effect output signal pulse width with display lines in unit
<table>
<tr><th>te_width[7:0]</th><th>Tearing Effect width(display line time)</th></tr>
<tr><td>0</td><td>1line time</td></tr>
<tr><td>1</td><td>2line time</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>N</td><td>N+1 line time</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>7f</td><td>128 line time</td></tr>
</table>
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0x00</td></tr>
<tr><td>SW Reset</td><td>0x00</td></tr>
<tr><td>HW Reset</td><td>0x00</td></tr>
</table></td></tr>
</table>

Flow Chart	TE Line Output OFF TEON(35h) 1st Parameter: M bit TE Line Output ON Command Parameter Display Action Mode Sequential transfer

4.3.5. Interface Control (F6h)

F6h	Interface Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
1st Parameter	1	1	1	XX	1	1	0	0	DM [1:0]		RM	RIM	C0

Description

DM [1:0]: Select the display operation mode.

DM[1]	DM[0]	Display Operation Mode
0	0	Internal clock operation
0	1	RGB Interface Mode
1	0	VSYNC interface Mode
1	1	Setting disabled

RM: Select the interface to access the GRAM.

Set RM to “1” when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

MDT[1:0] : Method of pixel data transfer. Please refer to section 4.5.6 Data Color Coding

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	(262K color)	6- bit RGB interface (3 transfer/pixel)

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	MDT[1:0]	DM [1:0]	RM	RIM
Power On Sequence	2’b00	2’b00	1’b0	1’b0

		SW Reset	2’b00	2’b00	1’b0	1’b0	
		HW Reset	2’b00	2’b00	1’b0	1’b0	

4.4. Description of Level 3 Command

4.4.1. Inversion (ECh)

<table>
<tr><td>ECh</td><td colspan="13">Inversion</td></tr>
<tr><td></td><td>D/C X</td><td>RD X</td><td>WR X</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>ECh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="3">DINV[2:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0x70</td></tr>
<tr><td>Description</td><td colspan="13">
DINV[2:0] : Set display inversion mode for dual gate （default）
<table>
<tr><th>DINV[2:0]</th><th>Inversion</th></tr>
<tr><td>0</td><td>1+2H1V</td></tr>
<tr><td>1</td><td>1+2 column</td></tr>
<tr><td>2</td><td>reserved</td></tr>
<tr><td>3</td><td>reserved</td></tr>
<tr><td>4</td><td>reserved</td></tr>
<tr><td>7</td><td>2 column inversion</td></tr>
</table>
DINV[2:0] : Set display inversion mode for single gate BFh=0x01
<table>
<tr><th>DINV[2:0]</th><th>Inversion</th></tr>
<tr><td>0</td><td>1dot</td></tr>
<tr><td>1/5/6/7</td><td>Column</td></tr>
<tr><td>2</td><td>reserved</td></tr>
<tr><td>3</td><td>reserved</td></tr>
<tr><td>4</td><td>reserved</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_ command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>DINV[2:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’h1</td></tr>
<tr><td>SW Reset</td><td>4’h1</td></tr>
<tr><td>HW Reset</td><td>4’h1</td></tr>
</table>
</td></tr>
</table>

4.4.2. Dual-Single gate select (BFh)

<table>
<tr><th>BFh</th><th colspan="13">Dual-Single gate</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>BFh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Dualgate</td><td>0x01</td></tr>
<tr><td>Description</td><td colspan="13">Dual gate :
Dualgate=1 select dual gate mode（default）
Dualgate=0 select single gate mode</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_ command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>Dualgate[1]</th></tr>
<tr><td>Power On Sequence</td><td>1’b1</td></tr>
<tr><td>SW Reset</td><td>1’b1</td></tr>
<tr><td>HW Reset</td><td>1’b1</td></tr>
</table>
</td></tr>
</table>

4.4.3. SPI 2DATA control(B1h)

B1h	SPI 2DATA control											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XX	X	X	X	X	2data_en	2data_mdt[2:0]			00

Description

2DATA_EN: Set 2_data_line mode in 3-wire/4-wire SPI.

2DATA_MDT[2:0] Set pixel data format in 2_data_line mode.

2DATA_MDT[2:0]	**Data Format**
000	65K color 1pixle/transition
001	262K color 1pixle/transition
010	262K color 2/3pixle/transition

Restriction

Inter command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	2DATA_EN	2DATA_MDT[2:0]
Power On Sequence	1’b0	3’b000
SW Reset	1’b0	3’b000
HW Reset	1’b0	3’b000

4.4.4. Power Control 1 (C1h)

<table>
<tr><th>C1h</th><th colspan="13">Power Control 1</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>vcire</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">vcire: Select the external reference voltage VDDB or internal reference voltage VDDBR.
<table>
<tr><td>vcire =0</td><td>Internal reference voltage 2.5V (default)</td></tr>
<tr><td>vcire =1</td><td>External reference voltage VDDB</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vcire</th></tr>
<tr><td>Power On Sequence</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>1’b0</td></tr>
</table></td></tr>
</table>

4.4.5. Power Control 2 (C3h)

<table>
<tr><th>C3h</th><th colspan="13">Power Control 2</th></tr>
<tr><td></td><td>D/C X</td><td>RD X</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>C3h</td></tr>
<tr><td>1^{st} Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="7">vreg1_vbp_d[6:0]</td><td>3C</td></tr>
<tr><td>Description</td><td colspan="13">
Set the voltage level value to output the VREG1A and VREG1B OUT level, which is a reference level for the grayscale voltage level.(Table is valid when vrh=0x28)
VREG1A=(vrh+vbp_d)*0.02+4
VREG1B=vbp_d*0.02+0.3
<table>
<tr><th>vreg1_vbp_d[6:0]</th><th>VREG1A/V</th><th>VREG1B/V</th></tr>
<tr><td>7'h00</td><td>4.8</td><td>0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>(N+40)*0.02+4</td><td>N*0.02+0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h55</td><td>6.5</td><td>2.0</td></tr>
<tr><td>7’h56</td><td>reserved</td><td>reserved</td></tr>
<tr><td>…</td><td>…</td><td></td></tr>
<tr><td>7’h7F</td><td>reserved</td><td>reserved</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vreg1_vbp_d[6:0]</th></tr>
<tr><td>Power On Sequence</td><td>7h3c</td></tr>
<tr><td>SW Reset</td><td>7h3c</td></tr>
<tr><td>HW Reset</td><td>7h3c</td></tr>
</table>
</td></tr>
</table>

4.4.6. Power Control 3 (C4h)

C4h	Power Control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
1st Parameter	1	1	↑	XX	X	vreg1_vbn_d[6:0]							3C

Description

Set the voltage level value to output the VREG2A OUT level, which is a reference level for the grayscale voltage level(Table is valid when vrh=0x28)

VREG2A=(vbn_d-vrh)*0.02-3.4

VREG2B=vbn_d*0.02+0.3

vreg1_vbn_d[6:0]	VREG2A/V	VREG2B/V
7'h00	-4.2	0.3
…	…	…
N	N*0.02-4.2	N*0.02+0.3
…	…	…
7'h55	-2.5	2.0
7'h56	reserved	reserved
…	…	…
7'h7F	reserved	reserved

Restriction

Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	vreg1_vbn_d[6:0]
Power On Sequence	7'h3C
SW Reset	7'h3C
HW Reset	7'h3C

4.4.7. Power Control 4 (C9h)

C9h	Power Control 4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
1st Parameter	1	1	↑	XX	X	X	vrh[5:0]						28
Description	Set the voltage level value to output the VREG1A OUT level, which is a reference level for the grayscale voltage level. (Table is valid when vbp_d=0x3C and vbn_d=0x3C) **VREG1A=(vrh+vbp_d)*0.02+4** **VREG2A=(vbn_d-vrh)*0.02-3.4**												
Restriction	Inter_command should be set high to enable this command												
Register Availability													
Default													

Description:

vrh[5:0]	VREG1A/V	VREG2A/V
6'h00	5.2	-2.2
…	…	…
N	(N+60)*0.02+4	(100-N)*0.02-4.2
…	…	…
6’h28	6	-3
…	…	…
6’h3F	6.46	-3.46

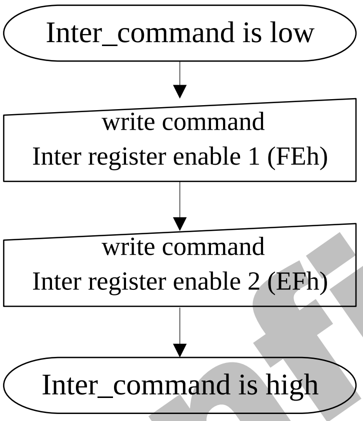
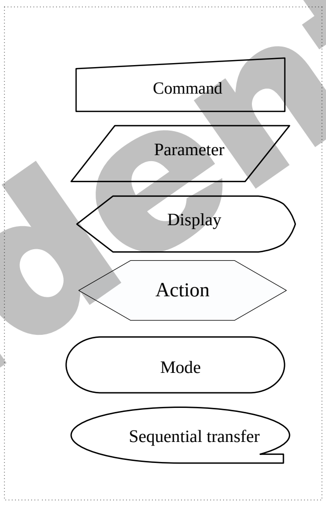
Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
	vrh[5:0]
Power On Sequence	6’h28
SW Reset	6’h28
HW Reset	6’h28

4.4.8. Inter Register Enable1(FEh)

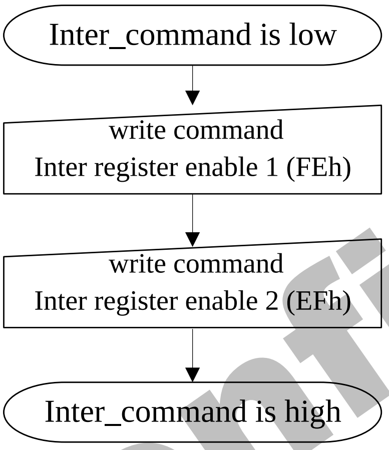
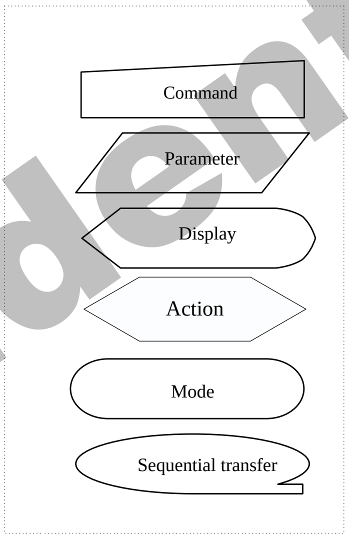
FEh	Inter register enable 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low.  Inter_command is low write command Inter register enable 1 (FEh) write command Inter register enable 2 (EFh) Inter_command is high  Command Parameter Display Action Mode Sequential transfer												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

4.4.9. Inter Register Enable2(EFh)

<table>
<tr><td>EFh</td><td colspan="13">Inter register enable 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>EFh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">
This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.

Inter_command is low
write command
Inter register enable 1 (FEh)
write command
Inter register enable 2 (EFh)
Inter_command is high

Command
Parameter
Display
Action
Mode
Sequential transfer
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

4.4.10. SET_GAMMA1 (F0h)

F0h	SET_GAMMA1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
1st Parameter	1	1	↑	XX	dig2gam_dig2j0_n[1:0]	dig2gam_vr1_n[5:0]							80
2nd Parameter	1	1	↑	XX	dig2gam_dig2j1_n[1:0]	dig2gam_vr2_n[5:0]							03
3st Parameter	1	1	↑	XX				dig2gam_vr4_n[4:0]					08
4nd Parameter	1	1	↑	XX				dig2gam_vr6_n[4:0]					06
5st Parameter	1	1	↑	XX	dig2gam_vr0_n[3:0]				dig2gam_vr13_n[3:0]				05
6nd Parameter	1	1	↑	XX		dig2gam_vr20_n[6:0]							2B
Description	dig2gam_dig2j0_n[1:0]: γ gradient adjustment register for negative polarity dig2gam_dig2j1_n[1:0]: γ gradient adjustment register for negative polarity dig2gam_vr0_n[3:0]: γ gradient adjustment register for negative polarity dig2gam_vr1_n[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr2_n[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr4_n[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr6_n[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr13_n[3:0]: γ gradient adjustment register for negative polarity dig2gam_vr20_n[6:0]: γ gradient adjustment register for negative polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

		Status	Default Value					
			dig2gam_dig2j0_n[1:0]	dig2gam_dig2j1_n[1:0]	dig2gam_vr0_n[3:0]	dig2gam_vr1_n[5:0]	dig2gam_vr2_n[5:0]	dig2gam_vr4_n[4:0]
Default		Power On Sequence	2’h02	2’h00	4’h00	6’h00	6’h03	5’h08
		SW Reset	2’h02	2’h00	4’h00	6’h00	6’h03	5’h08
		HW Reset	2’h02	2’h00	4’h00	6’h00	6’h03	5’h08

		Status	Default Value					
			dig2gam_vr6_n[4:0]	dig2gam_vr13_n[3:0]	dig2gam_vr20_n[6:0]			
Default		Power On Sequence	5’h06	4’h05	7’h2b			
		SW Reset	5’h06	4’h05	7’h2b			
		HW Reset	5’h06	4’h05	7’h2b			

4.4.11. SET_GAMMA2 (F1h)

F1h	SET_GAMMA2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
1st Parameter	1	1	↑	XX		dig2gam_vr43_n[6:0]							41
2nd Parameter	1	1	↑	XX	dig2gam_vr27_n[2:0]			dig2gam_vr57_n[4:0]					97
3st Parameter	1	1	↑	XX	dig2gam_vr36_n[2:0]			dig2gam_vr59_n[4:0]					98
4nd Parameter	1	1	↑	XX			dig2gam_vr61_n[5:0]						13
5st Parameter	1	1	↑	XX			dig2gam_vr62_n[5:0]						17
6nd Parameter	1	1	↑	XX	dig2gam_vr50_n[3:0]				dig2gam_vr63_n[3:0]				CD
Description	dig2gam_vr43_p[6:0]: γ gradient adjustment register for negative polarity dig2gam_vr27_p[2:0]: γ gradient adjustment register for negative polarity dig2gam_vr57_p[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr59_p[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr36_p[2:0]: γ gradient adjustment register for negative polarity dig2gam_vr61_p[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr62_p[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr50_p[3:0]: γ gradient adjustment register for negative polarity dig2gam_vr63_p[3:0]: γ gradient adjustment register for negative polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

	Status	Default Value					
		dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr59_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr61_p[5:0]
Default	Power On Sequence	7’h41	3’h04	5’h17	5’h18	3’h04	6’h13
	SW Reset	7’h41	3’h04	5’h17	5’h18	3’h04	6’h13
	HW Reset	7’h41	3’h04	5’h17	5’h18	3’h04	6’h13

	Status	Default Value					
		dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Default	Power On Sequence	6’h17	4’h0C	4’h0D			
	SW Reset	6’h17	4’h0C	4’h0D			
	HW Reset	6’h17	4’h0C	4’h0D			

4.4.12. SET_GAMMA3 (F2h)

F2h	SET_GAMMA3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
1st Parameter	1	1	↑	XX	dig2gam_dig2j0_p[1:0]		dig2gam_vr1_p[5:0]						40
2nd Parameter	1	1	↑	XX	dig2gam_dig2j1_p[1:0]		dig2gam_vr2_p[5:0]						03
3st Parameter	1	1	↑	XX				dig2gam_vr4_p[4:0]					08
4nd Parameter	1	1	↑	XX				dig2gam_vr6_p[4:0]					0B
5st Parameter	1	1	↑	XX	dig2gam_vr0_p[3:0]				dig2gam_vr13_p[3:0]				08
6nd Parameter	1	1	↑	XX		dig2gam_vr20_p[6:0]							2E
Description	dig2gam_dig2j0_p[1:0]: γ gradient adjustment register for positive polarity dig2gam_dig2j1_p[1:0]: γ gradient adjustment register for positive polarity dig2gam_vr1_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr2_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr4_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr6_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr0_p[3:0]: γ gradient adjustment register for positive polarity dig2gam_vr13_p[3:0]: γ gradient adjustment register for positive polarity dig2gam_vr20_p[6:0]: γ gradient adjustment register for positive polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

	Status	Default Value					
		dig2gam_dig2j0_p[1:0]	dig2gam_dig2j1_p[1:0]	dig2gam_vr1_p[5:0]	dig2gam_vr2_p[5:0]	dig2gam_vr4_p[4:0]	dig2gam_vr6_p[4:0]
Default	Power On Sequence	2’h01	2’h00	6’h00	6’h03	5’h08	5’h0B
	SW Reset	2’h01	2’h00	6’h00	6’h03	5’h08	5’h0B
	HW Reset	2’h01	2’h00	6’h00	6’h03	5’h08	5’h0B

	Status	Default Value					
		dig2gam_vr0_p[3:0]	dig2gam_vr13_p[3:0]	dig2gam_vr20_p[6:0]			
Default	Power On Sequence	4’h00	4’h08	7’h2E			
	SW Reset	4’h00	4’h08	7’h2E			
	HW Reset	4’h00	4’h08	7’h2E			

4.4.13. SET_GAMMA4 (F3h)

F3h	SET_GAMMA4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h
1st Parameter	1	1	↑	XX		dig2gam_vr43_p[6:0]							3F
2nd Parameter	1	1	↑	XX	dig2gam_vr27_p[2:0]			dig2gam_vr57_p[4:0]					98
3st Parameter	1	1	↑	XX	dig2gam_vr36_p[2:0]			dig2gam_vr59_p[4:0]					B4
4nd Parameter	1	1	↑	XX			dig2gam_vr61_p[5:0]						14
5st Parameter	1	1	↑	XX			dig2gam_vr62_p[5:0]						18
6nd Parameter	1	1	↑	XX	dig2gam_vr50_p[3:0]				dig2gam_vr63_p[3:0]				CD
Description	dig2gam_vr43_p[6:0]: γ gradient adjustment register for positive polarity dig2gam_vr27_p[2:0]: γ gradient adjustment register for positive polarity dig2gam_vr57_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr36_p[2:0]: γ gradient adjustment register for positive polarity dig2gam_vr59_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr61_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr62_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr50_p[3:0]: γ gradient adjustment register for positive polarity dig2gam_vr63_p[3:0]: γ gradient adjustment register for positive polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Avail bility
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

	Status	Default Value					
		dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr59_p[4:0]	dig2gam_vr61_p[5:0]
Default	Power On Sequence	7’h3F	3’h04	5’h18	3’h05	5’h14	6’h14
	SW Reset	7’h3F	3’h04	5’h18	3’h05	5’h14	6’h14
	HW Reset	7’h3F	3’h04	5’h18	3’h05	5’h14	6’h14

	Status	Default Value					
		dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Default	Power On Sequence	6’h18	4’h0C	4’h0D			
	SW Reset	6’h18	4’h0C	4’h0D			
	HW Reset	6’h18	4’h0C	4’h0D			

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9D01N is used out of the absolute maximum ratings, GC9D01N may be permanently damaged. To use GC9D01N within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9D01N will malfunction and cause poor reliability.

Table43.

Item	Symbol	Unit	Value
Supply voltage	VDDB	V	-0.3~+4.6
Supply voltage(Logic)	VDDI	V	-0.3~+4.6
Supply voltage(Digital)	DVDD	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+27.0
Logic input voltage range	VIN	V	-0.3~VDDI+0.3
Logic output voltage range	VO	V	-0.3~VDDI+0.3
Operation temperature	Topr	℃	-40~+80
Storage temperature	Tstg	℃	-40~+80
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

5.2. DC Characteristics

5.2.1. DC Characteristics for Panel Driving

General DC Characteristics

Table44.

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VDDB	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	DVDD	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	9.0	-	14.0	Note3
Gate Driver Low Voltage	VGL	V	-	-14.0	-	-9.0	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSSB	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSSB	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSSB	-0.1	-	+0.1	Note1,2,3
Source Driver							
Positive Source Output Range	Vsout	V	-	VREG1B	-	VREG1A	
Negative Source Output Range	Vsout	V	-	VREG2A	-	VREG2B	

Note 1: VDDI=1.65 to 3.3V, VDDB=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital VDDI voltage equal or less than analog VDDB voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,IM0, and Test pins.

5.3. AC Characteristics

5.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅰ)

Figure90.

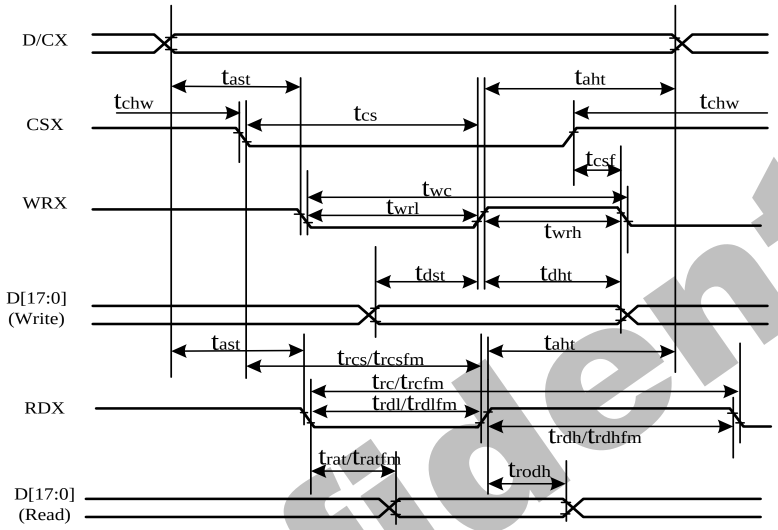

D/CX
CSX
WRX
D[17:0]
(Write)
RDX
D[17:0]
(Read)
tast
taht
tchw
tcs
tchw
tcsf
twc
twrl
twrh
tdst
tdht
tast
trcs/trcsfm
taht
trc/trcfm
trdl/trdlfm
trdh/trdhfm
trat/tratfm
trodh

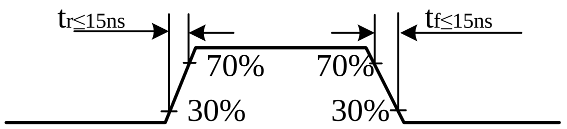
Table45.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[17:0],D[15:0],D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	

	tratfm	Read access time	-	340	ns	CL=8pF
	trod	Read output disable time	20	80	ns	

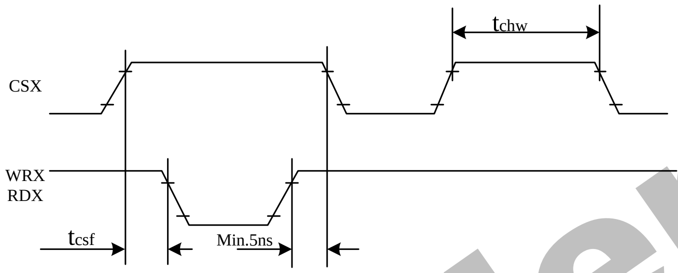
Note: Ta = -40 to 85 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSS=0V

Figure91.


tr≤15ns
tf≤15ns
70%
70%
30%
30%

CSX timings :

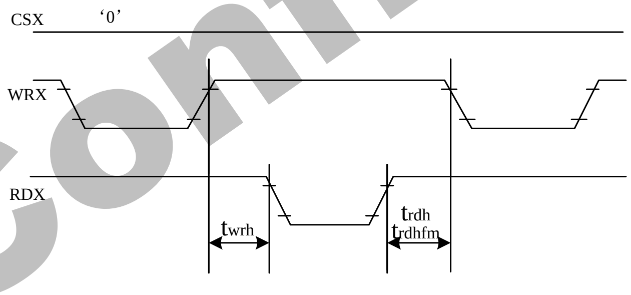
Figure92.


tchw
CSX
WRX
RDX
tcsf
Min.5ns

Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

Figure92.


CSX
'0'
WRX
RDX
twrh
trdh
trdhfm

Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅱ)

Figure93.

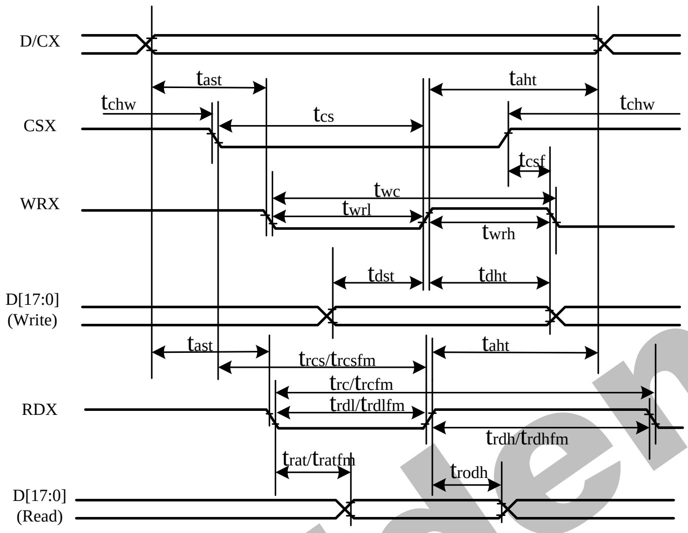
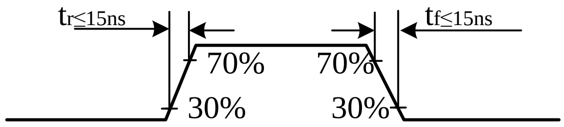

D/CX
CSX
WRX
D[17:0]
(Write)
RDX
D[17:0]
(Read)
tast
taht
tchw
tcs
tchw
tcsf
twc
twrl
twrh
tdst
tdht
tast
taht
trcs/trcsfm
trc/trcfm
trdl/trdlfm
trdh/trdhfm
trat/tratfm
trodh

Table46.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	70	-	ns	
D[17:0], D[17:10] &D[8:1], D[17:10] ,D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

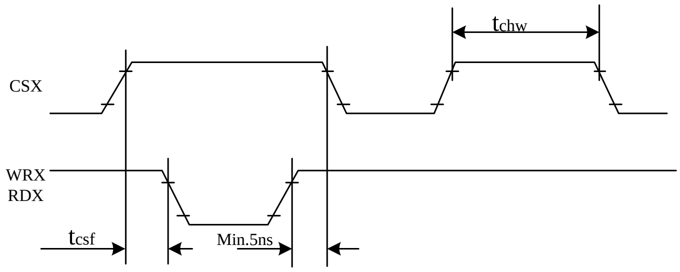
Note: Ta = -40 to 85 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSS=0V.

Figure94.


tr≤15ns
tf≤15ns
70%
70%
30%
30%

CSX timings :

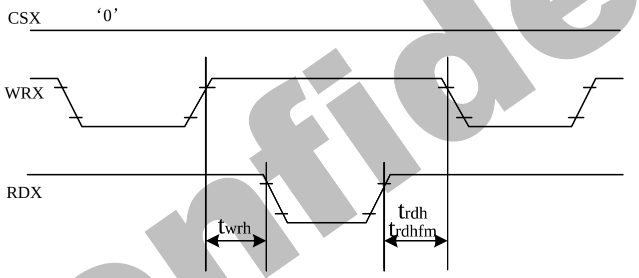
Figure95.


tchw
CSX
WRX
RDX
tcsf
Min.5ns

Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

Figure96.


CSX
'0'
WRX
RDX
twrh
trdh
trdhfm

Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

Figure97.

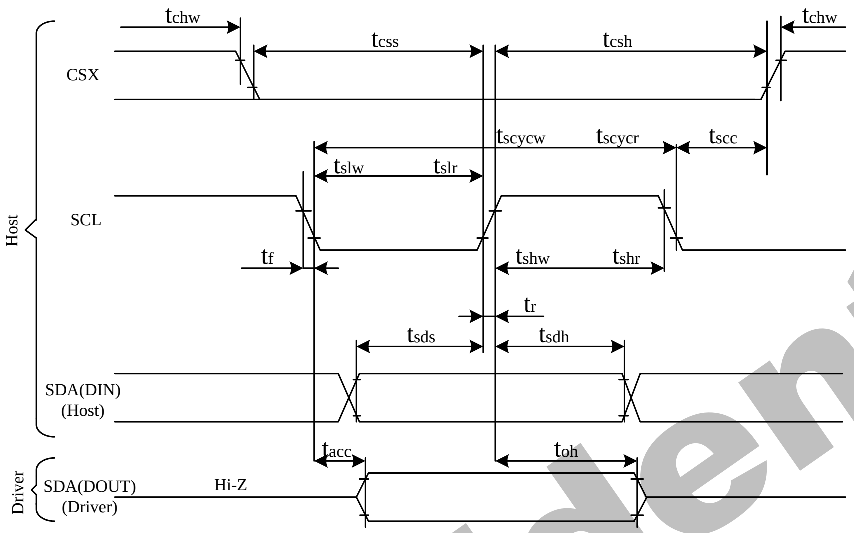
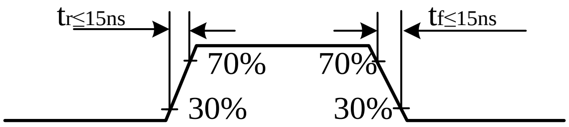

tchw
tcss
tcsh
tchw
CSX
tscycw
tscycr
tscc
tslw
tslr
Host
SCL
tf
tshw
tshr
tr
tsds
tsdh
SDA(DIN)
(Host)
tacc
toh
Driver
SDA(DOUT)
(Driver)
Hi-Z

Table47.

Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0(Outp)	tacc	Access time (Read)	10	-	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	20	-	ns	
	tcsh		40	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, VSSB=VSSB=0V

Figure98.


tr≤15ns
tf≤15ns
70%
70%
30%
30%

5.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)

Figure98.

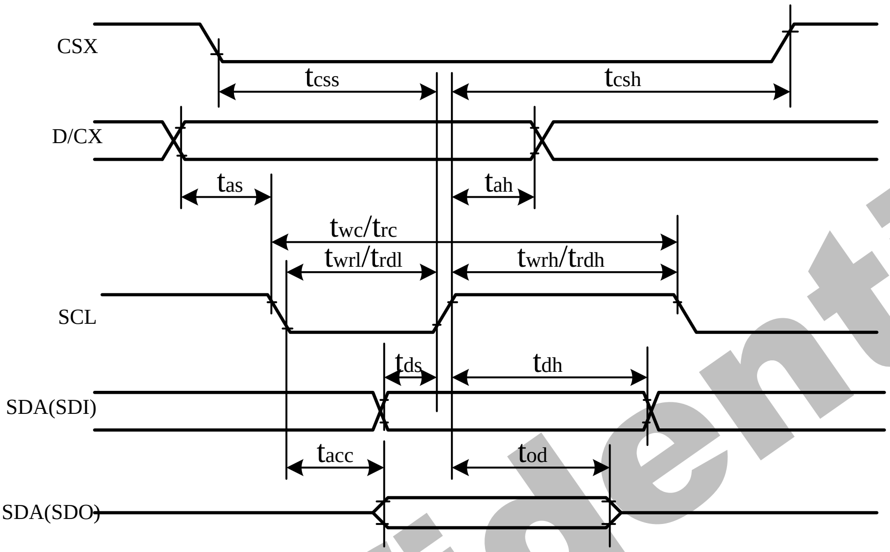
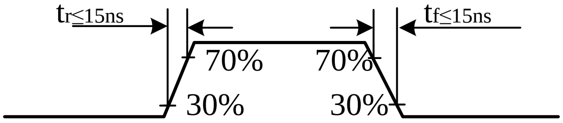

CSX
tcss
tcsh
D/CX
tas
tah
twc/trc
twrl/trdl
twrh/trdh
SCL
tds
tdh
SDA(SDI)
tacc
tod
SDA(SDO)

Table48.

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, AGND=VSS=0V

Figure99.


tr≤15ns
tf≤15ns
70%
70%
30%
30%

5.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics

Figure100.

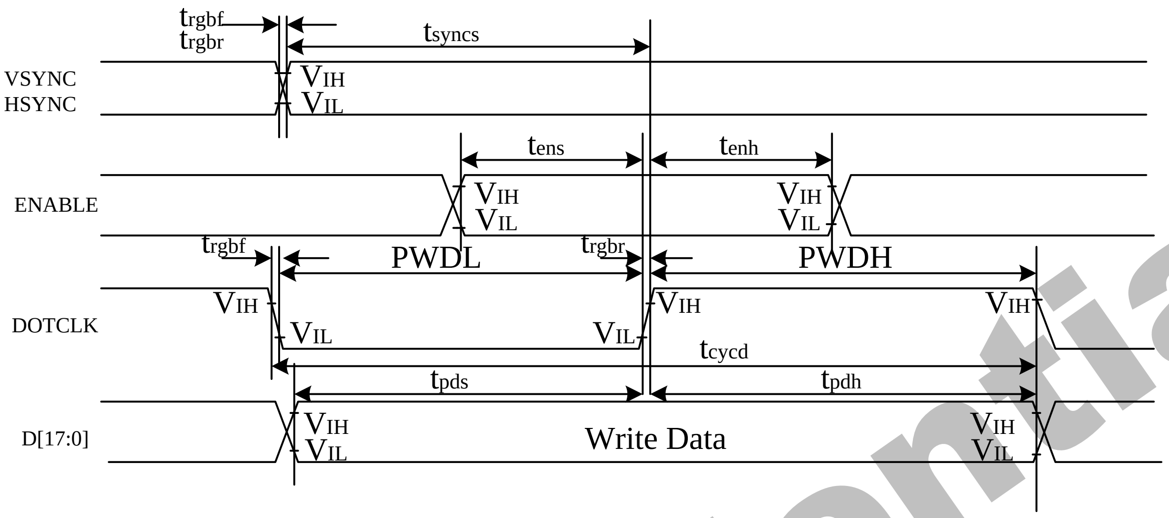
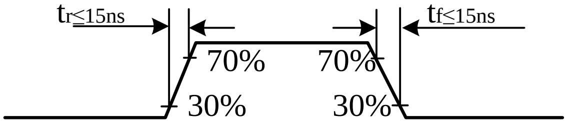

trgbf
trgbr
tsyncs
VSYNC
HSYNC
VIH
VIL
tens
tenh
ENABLE
VIH
VIL
VIH
VIL
trgbf
PWDL
trgbr
PWDH
DOTCLK
VIH
VIL
VIL
VIH
VIH
tcycd
tpds
tpdh
D[17:0]
VIH
VIL
Write Data
VIH
VIL

Table49.

Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDDB=2.5V to 3.3V, AGND=VSS=0V

Figure101.


tr≤15ns
tf≤15ns
70%
70%
30%
30%