CV180xB
4-Layer PCB 38x38mm2
Layout Guide

Version: 0.2

Release date: 2022/10/13

Outline

- Checklist
- Stackup
- DDR 电源绕线
- Serdes讯号绕线
  - MIPI/USB/EPHY
- Single-end讯号绕线
  - GPIO/SDIO
  - EMMC/AUD/XTAL/WIFI
- 模拟/数字电源绕线
  - VDDC
  -模拟IO电源

CV180xB PCB Type

- 4-Layer PCB 38x38mm2 layout 支持以下IC型号:
  - QFN68 PKG: CV1800B/CV1801B/CV1802B, DDR2/DDR3 SIP on PKG

  Note: PCB 限定板形尺寸38x38mm2

- Layout rule 分成以下两部份:
  (1) **DDR Layout rule**
  (2) **Serdes/Single-end/Power Layout rule**

- QFN PKG 与叠构相对应PCB layout rule如下:

Type	Stackup	DDR layout rule	Serdes/Single-end/Power Layout rule
QFN PKG	4-Layer PCB (size 38x38mm2)	QFN 电源绕线	4-layer PCB layout rule

Checklist

Checklist – Stackup – 4L-PCB

No.	Rule	Description	Requirement	Check
1	4L-PCB 叠构要求	介电层/铜 厚度限制	1. 确认介电层厚度 – pp/core (1) pp<=5mils (Cu与pp 压合后, pp不含Cu的厚度) (2) L2/L3 Core 厚度>=25mils, 2. 每层Cu厚度1oz.	

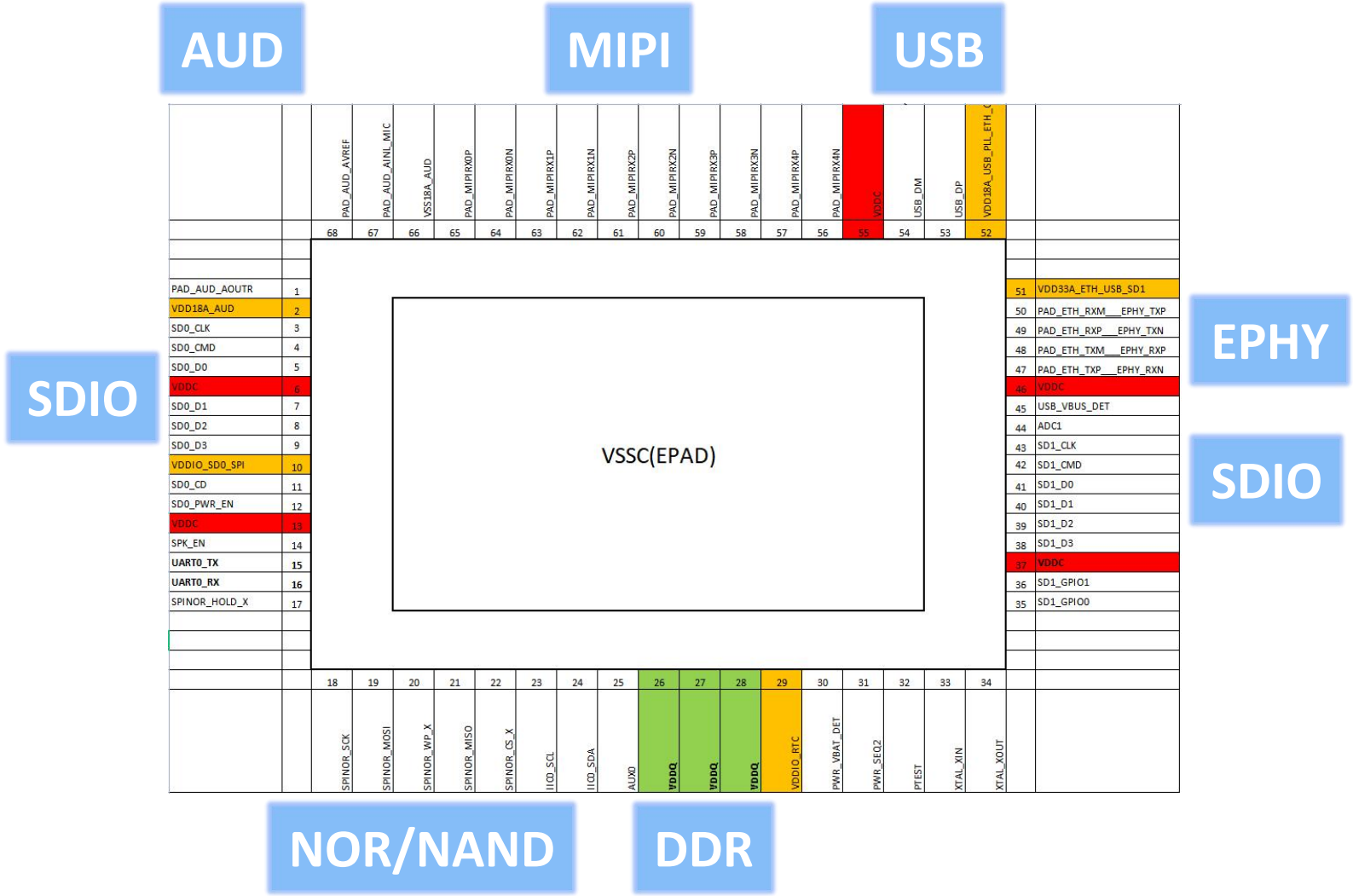
Checklist - Layout rule

No.	Rule	Description	Requirement	Check
1	DDR routing	DDR3Q_1.35V rule	1. 确认QFN PKG E-pad solder mask 覆盖区 (5.7x5.7mm2) 2 颗VIA 2. 建议贴上SOC PKG 下方DDR 走线/VIA/Cap layout	
2	MIPI routing	表层/内层 阻抗控制	与PCB vendor 确认polar 结果: (1) 表层: Diff Coated Coplanar Strips with GND 1B (2) 内层: Diff Offset Coplanar Strips 1B1A	
3		表层走线 Lane to lane NO GND shielding	Lane to lane NO GND shielding 走线长度<3.5mm	
4		Length matching rule	确认TX/RX length matching	
5	USB	表层/内层 阻抗控制	与PCB vendor 确认polar 结果: (1) 表层: Diff Coated Coplanar Strips with GND 1B (2) 内层: Diff Offset Coplanar Strips 1B1A	
6		Length matching rule	P/N length matching	
7	EPHY routing	表层/内层 阻抗控制	与PCB vendor 确认polar 结果: (1) 表层: Diff Coated Coplanar Strips with GND 1B (2) 内层: Diff Offset Coplanar Strips 1B1A	
8		Length matching rule	P/N length matching	

Checklist - Layout rule

No.	Rule	Description	Requirement	Check
9	Single-end rule	表层/内层 shielding rule	Shielding rule	
10	NOR/NAND rule	表层/内层 shielding rule	Shielding rule	
11	AUD rule	表层 shielding rule	Shielding rule	
12	XTAL rule	表层 shielding rule	Shielding rule	
13	RTC rule	表层 shielding rule	Shielding rule	
14	WIFI_ANT rule	表层阻抗控制	与PCB vendor 确认polar 结果: (1) 表层: Coated Coplanar Strips with GND 1B	
15	VDC rule	1. 确认Cap数量与位置, VIA数量 2. 通道宽度	1. Rule1: (1) SOC/PMIC 处VIA 数量 (2) SOC处Cap pin VDDC/GND VIA rule 2. 通道宽度参照 rule2 3. 建议贴上SOC PKG 下方VDDC 走线/VIA/Cap layout	
16	Analog IO Power rule	1. 线宽rule 2. 确认Cap数量与位置, VIA数量	1. Rule1: (1) SOC/PMIC 处VIA 数量 (2) SOC处Cap pin power/GND VIA rule 2. 通道宽度参照 rule2 3. 建议贴上SOC PKG 下方power走线/VIA/Cap layout	

QFN Ball Map


AUD
MIPI
USB
SDIO
EPHY
SDIO
NOR/NAND
DDR
VSSC(EPAD)
1 PAD_AUD_AOUTR
2 VDD18A_AUD
3 SD0_CLK
4 SD0_CMD
5 SD0_D0
6 VDDC
7 SD0_D1
8 SD0_D2
9 SD0_D3
10 VDDIO_SD0_SPI
11 SD0_CD
12 SD0_PWR_EN
13 VDDC
14 SPK_EN
15 UART0_TX
16 UART0_RX
17 SPINOR_HOLD_X
18 SPINOR_SCK
19 SPINOR_MOSI
20 SPINOR_WP_X
21 SPINOR_MISO
22 SPINOR_CS_X
23 IIC0_SCL
24 IIC0_SDA
25 AUX0
26 VDDQ
27 VDDQ
28 VDDQ
29 VDDIO_RTC
30 PWR_VBAT_DET
31 PWR_SEQ2
32 PTEST
33 XTAL_XIN
34 XTAL_XOUT
35 SD1_GPIO0
36 SD1_GPIO1
37 VDDC
38 SD1_D3
39 SD1_D2
40 SD1_D1
41 SD1_D0
42 SD1_CMD
43 SD1_CLK
44 ADC1
45 USB_VBUS_DET
46 VDDC
47 PAD_ETH_TXP___EPHY_RXN
48 PAD_ETH_TXM___EPHY_RXP
49 PAD_ETH_RXP___EPHY_TXN
50 PAD_ETH_RXM___EPHY_TXP
51 VDD33A_ETH_USB_SD1
52 VDD18A_USB_PLL_ETH_C
53 USB_DP
54 USB_DM
55 VDDC
56 PAD_MIPIRX4N
57 PAD_MIPIRX4P
58 PAD_MIPIRX3N
59 PAD_MIPIRX3P
60 PAD_MIPIRX2N
61 PAD_MIPIRX2P
62 PAD_MIPIRX1N
63 PAD_MIPIRX1P
64 PAD_MIPIRX0N
65 PAD_MIPIRX0P
66 VSS18A_AUD
67 PAD_AUD_AINL_MIC
68 PAD_AUD_AVREF

Stackup

QFN PKG: CV1800B/CV1801B/CV1802B

PCB 4-Layer Stackup

- 叠构层数: 4层
- 叠构厚度: 1mm +/-10% <=厚度 <=1.6mm +/-10%
- 每层Cu采用1oz.
- 介电层厚度限制:

层号	材质	厚度限制
L1/L2	Prepreg	<=5mils (Cu与pp 压合后, pp不含cu厚度)
L3/L4		
L2/L3	Core	>=25mils

参考叠构

Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

DDR 电源绕线 (DDR3_1.35V)

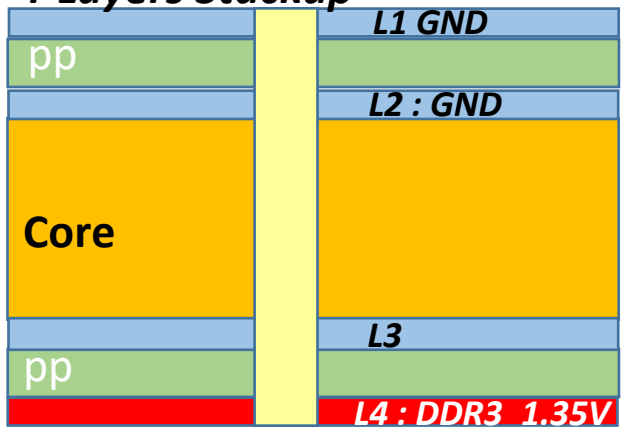
QFN PKG: CV1800B/CV1801B/CV1802B

4-Layer PCB (38x38mm2)

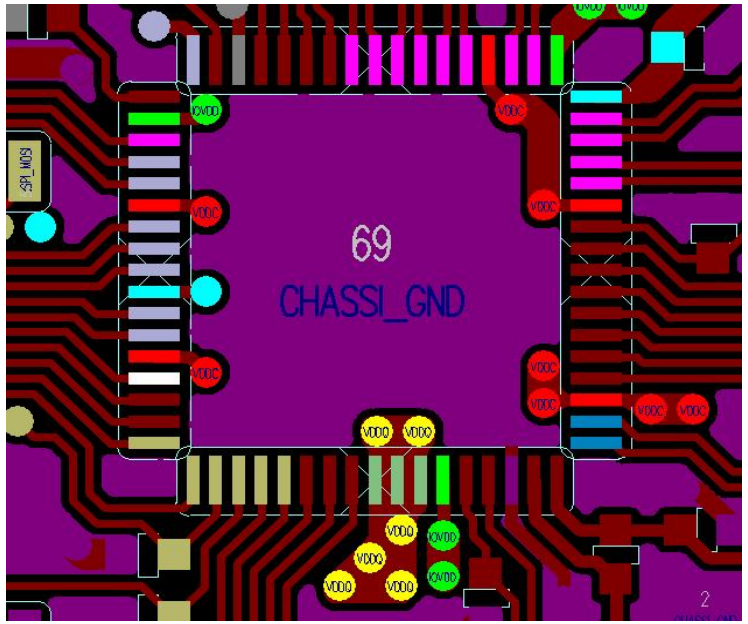
QFN – 4L-PCB DDR Layout

- Stackup:
  (1) GND@L2(shape)
  (2) DDR3_1.35V@L1/L2 (shape)

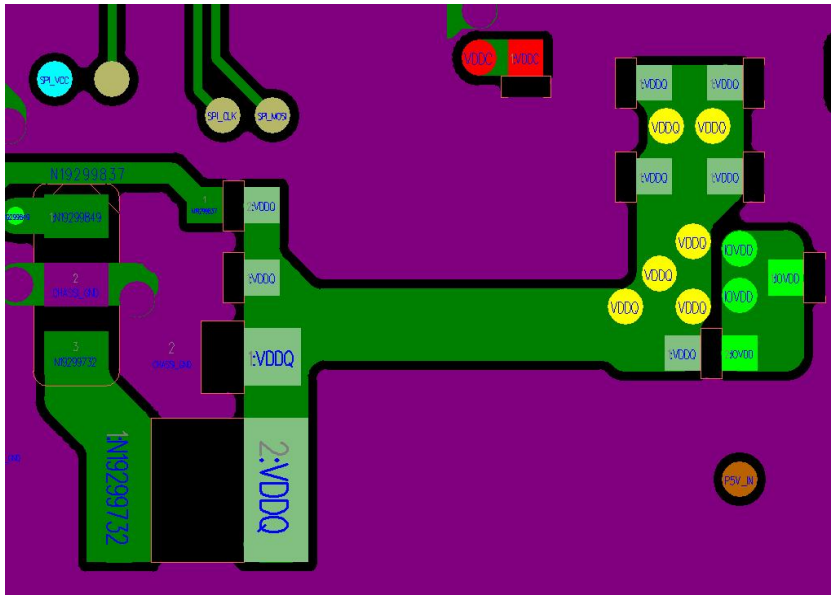
4-Layers Stackup



DDR3_1.35V@Top



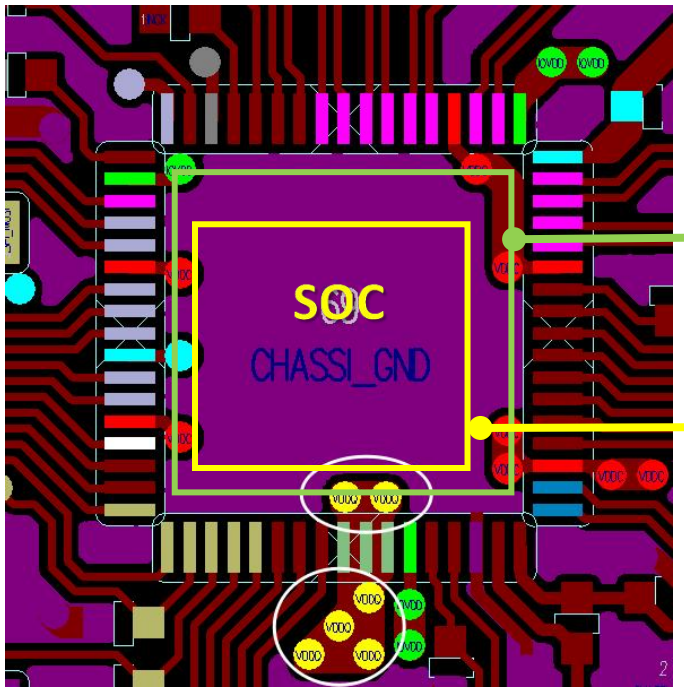
DDR3_1.35V@Bottom



QFN - 4L-PCB - DDR3_1.35V - Rule 1

Power	Layer	SOC VIA count	Layout rule
DDR3_1.35V	Top	(1) @E-pad 5.7x5.7mm2区域: VIA 数量: 2 (2) pin out区域: VIA 数量: 4	(1) 覆盖Solder mask区域: E-pad 5.7x5.7mm2 (2) 非覆盖Solder mask区域: E-pad 4x4mm2 (3) 确认DDR3_1.35V SOC 端VIA数量

DDR3_1.35V@Top



E-pad aera 5.7x5.7mm2 (solider mask)

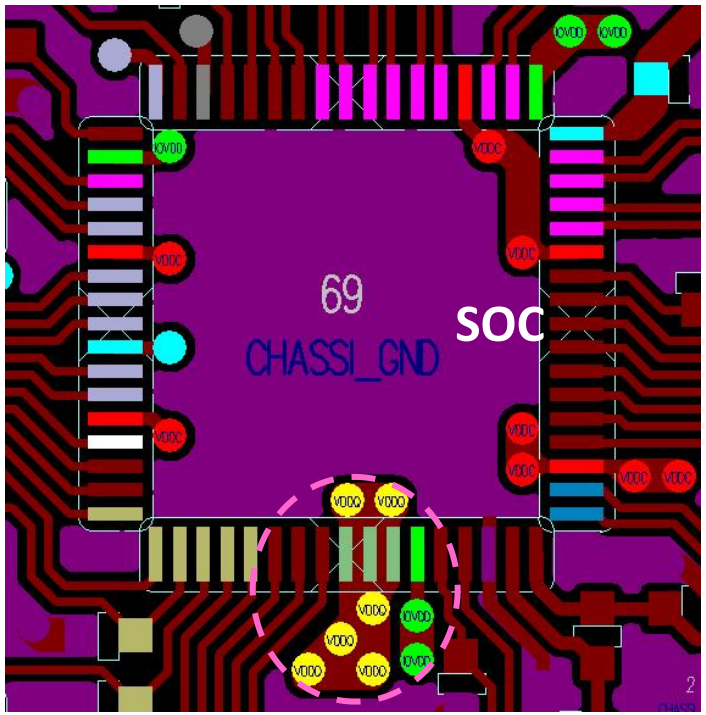
E-pad aera 4x4mm2 (uncover solider mask)

pin out区域

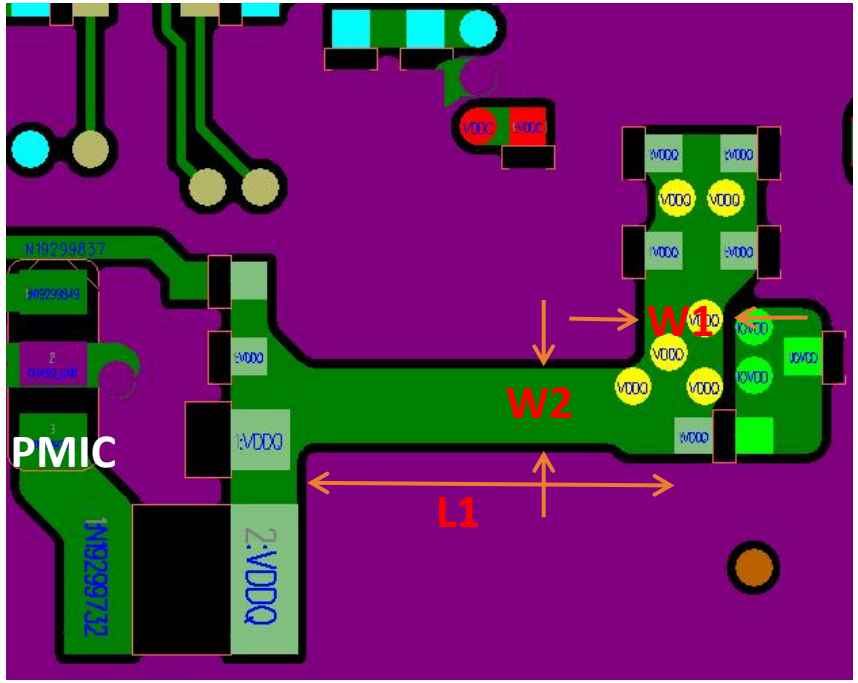
QFN - 4L-PCB DDR3 – DDR3_1.35V - Rule 2

Power	Layer	Layout rule
DDR3_1.35V	Bottom	DDR3_1.35V main route, (1) 确认SOC处有下6颗VIA (2) 尺寸要求: 1) W1>=1.5mm 2) L1<=10mm, , 扣除破孔有效宽度: W2>=1mm **(板形<=38x38mm2)** **3) L1>10mm, 扣除破孔有效宽度: W2>=1.5mm (板形>38x38mm2)**

DDR3_1.35V@Top



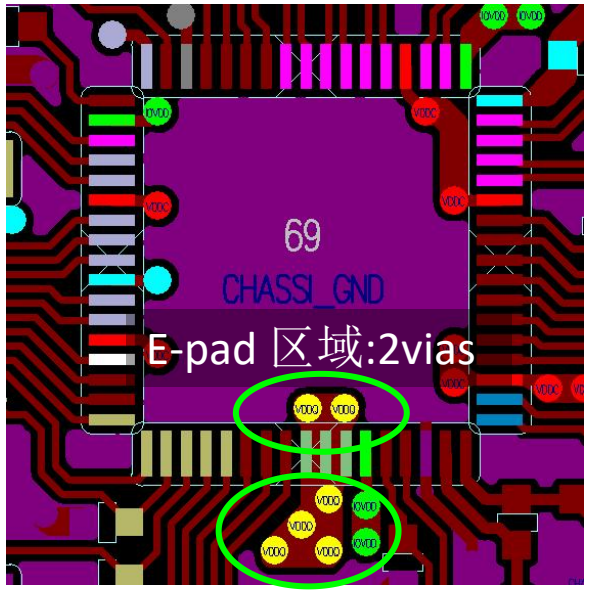
DDR3_1.35V@Bottom



QFN - 4L-PCB - DDR3Q_1.35V - Rule 3

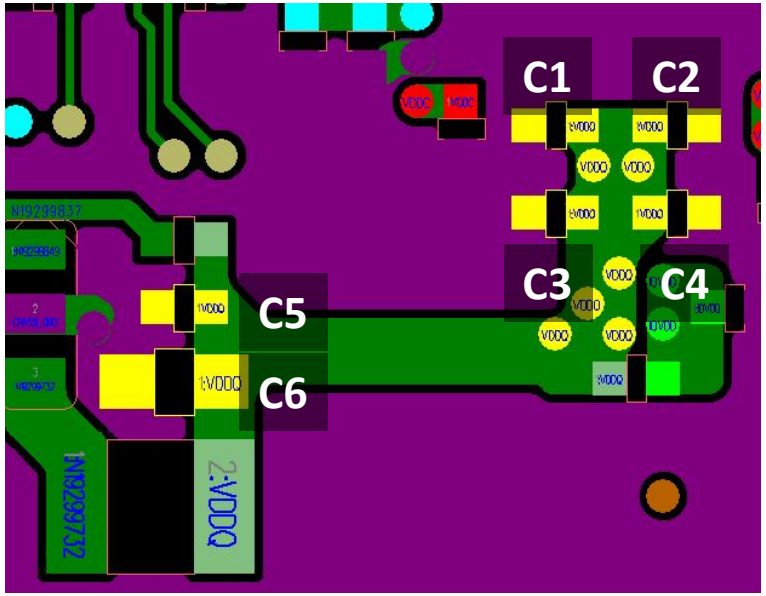
Power	Layer	DeCap@Dram area	Layout rule
DDR3Q_1.35V	Top/Bottom	DDR3Q_1.35V@Bottom: (1) 0402 0.1uF: C2 /C4 (2) 0402 1uF: C1 (3) 0402 4.7uF: C3/C5 (4) 0603 10uF: C6	(1) DDR3_1.35V VIA rule E-pad 区域 2颗via紧连C1/C2 Pin-out 区域 4颗 via紧连C3/C4/C5/C6 (1) GND VIA rule 确认每颗Cap旁至少1颗GND via

DDR3_1.35V@Top



Pin-out 区域:4 vias

DDR3_1.35V@Bottom



Serdes 讯号绕线

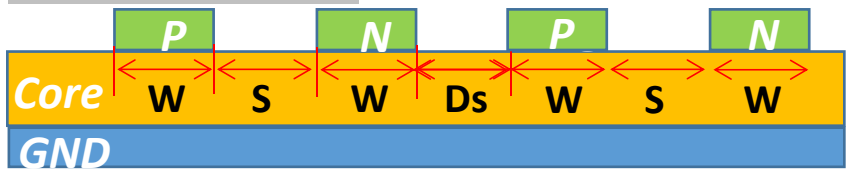
QFN PKG: CV1800B/CV1801B/CV1802B

4-Layer

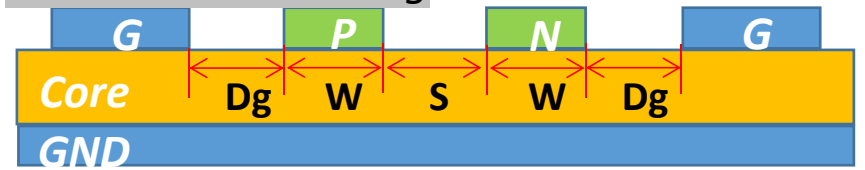
QFN 4L-PCB – MIPI Routing – 表层走线

Signal	Layer	Zo	Shielding Rule	Trace width/spacing (mm)
MIPI RX Diff pair	Top/ Bottom	100 ohm	(1) Routing length L1<=3.5mm **NO GND shielding**	(1) 0.125/0.1(W/S) (2) Ds>=0.2 (lane to lane spacing)
			(2) Routing length L1>3.5mm **Lane to lane shielding**	0.125/0.125/0.125 (W/S/Dg)

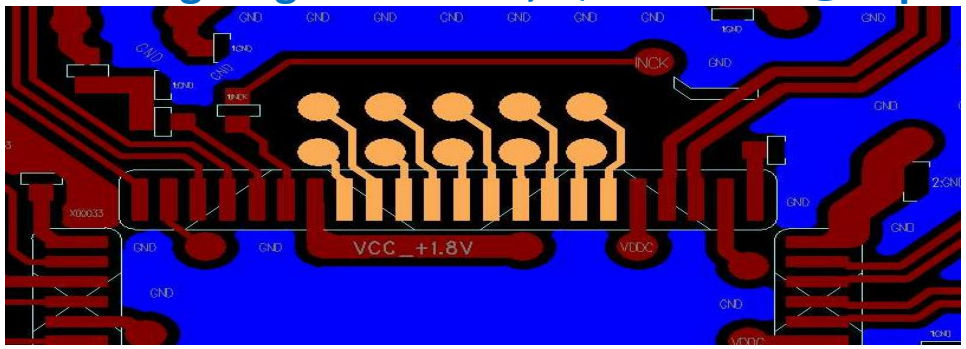
NO GND shielding



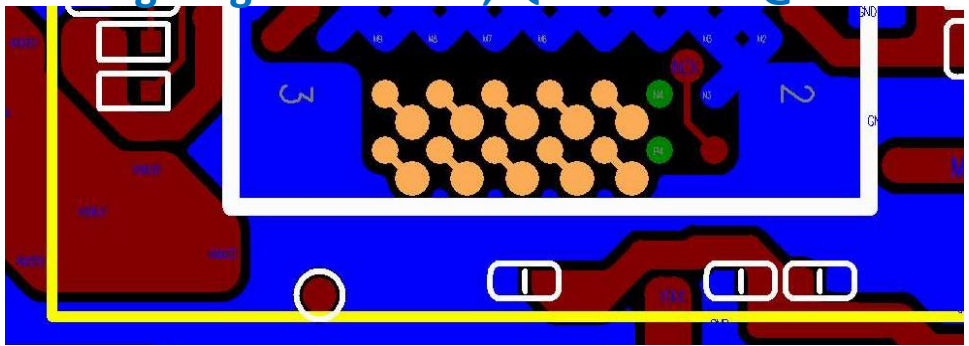
Lane to lane shielding



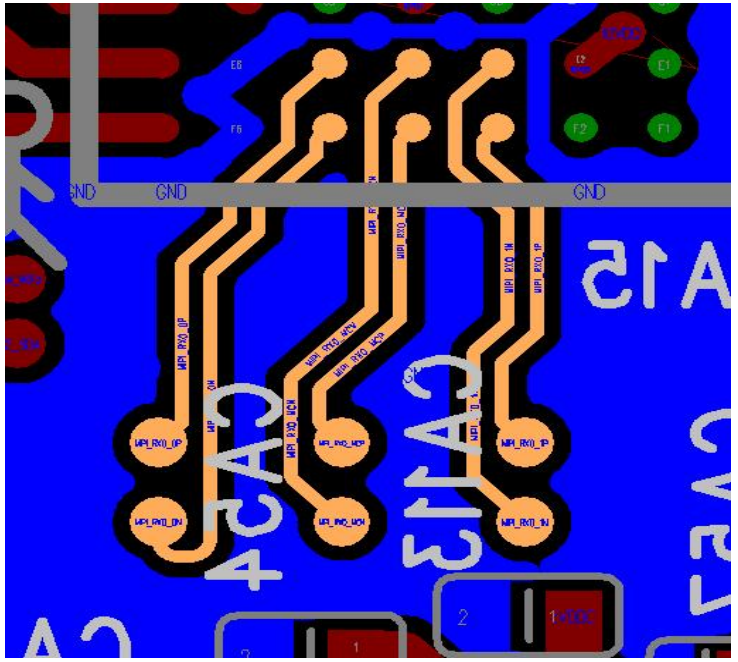
Routing length<=3.5mm, QFN MIPI RX@Top



Routing length<=3.5mm, QFN MIPI RX@Bottom



Routing length>=3.5mm, QFN MIPI RX@Bottom



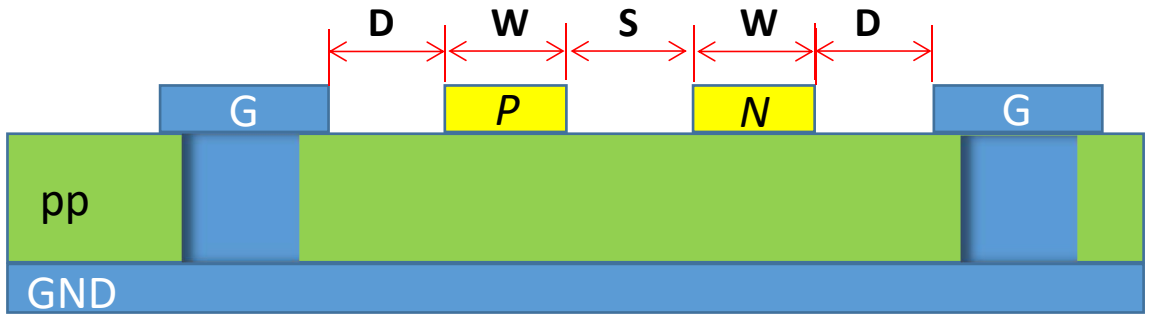
MIPI Routing – Length Matching Rule

Signal	Matching Reference	Matching Length
TX	inter skew	<=2.5mm (100mils)
RX	inter skew	
TX	P/N intra skew	<=0.5mm (20mils)
RX	P/N intra skew	

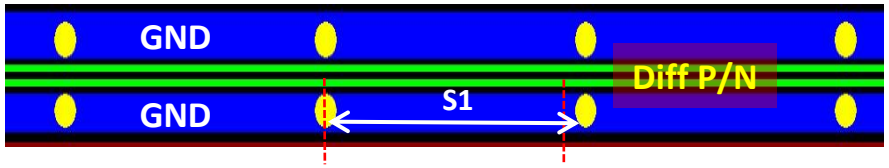
QFN – 4L-PCB – USB Routing – 表层走线- Rule

Signal	Layer	Zo	Trace width/spacing (mm)	Shielding Rule
USB Diff pair	Top/ Bottom	90ohm	0.125/0.1/0.15 (W/S/D)	(1) Lane to lane GND shielding. (2) Shielding GND VIA: Lane to Lane GND shielding必须下VIA (VIA to VIA 距离<=7.5mm)

USB Diff pair



Shielding GND VIA



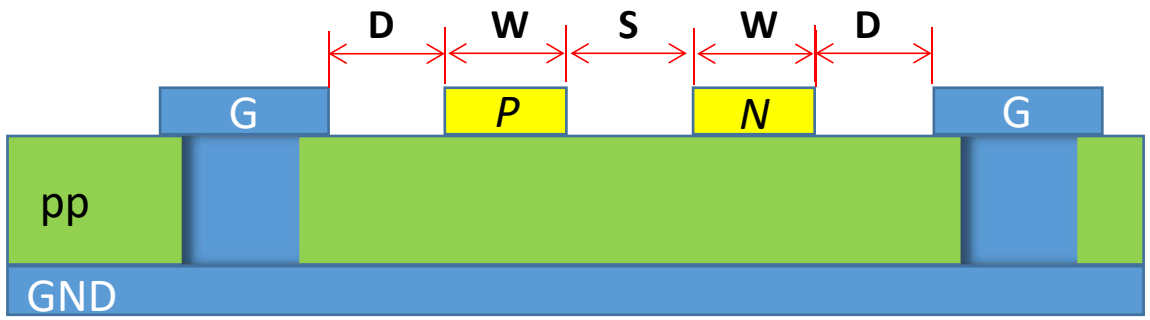
USB Routing – Length Matching Rule

Signal	Matching Reference	Matching Length
USB_DM **USB_DP**	P/N intra skew	<=0.5mm (20mils)

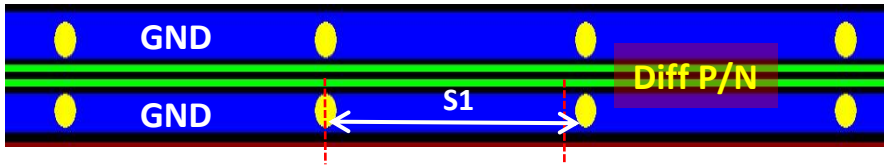
QFN – 4L-PCB - EPHY Routing – 表层走线 – 线长<=40mm

Signal	Layer	Zo	Trace width/spacing (mm)	Shielding Rule
EPHY TX/RX Diff pair	Top	100ohm	0.125/0.125/0.15 (W/S/D)	(1) Lane to lane GND shielding. (2) Shielding GND VIA: Lane to Lane GND shielding必须下VIA (VIA to VIA 距离 S1<=7.5mm)

EPHY TX/RX



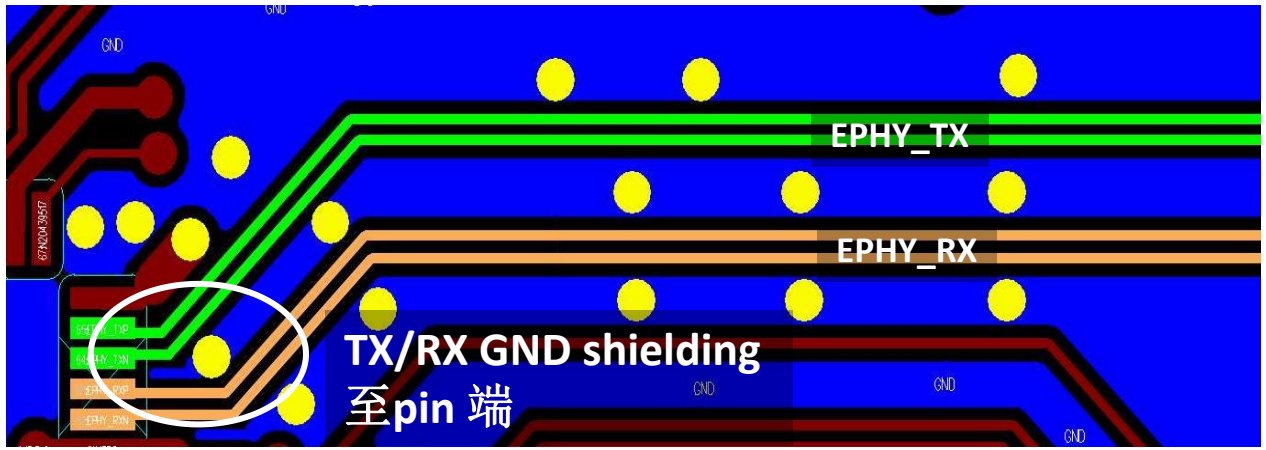
Shielding GND VIA



QFN 4L-PCB EPHY Routing –表层走线 – 线长<=40mm

Signal	Layer	Requirement	Layout Rule
EPHY TX/RX	Top	TX to RX GND shielding	确认TX/RX GND shielding至pin/ball 端

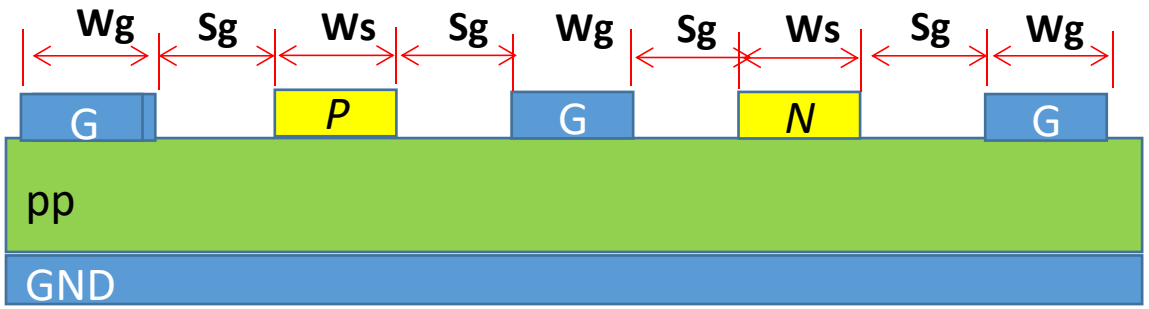
QFN EPHY TX/RX differential@L1



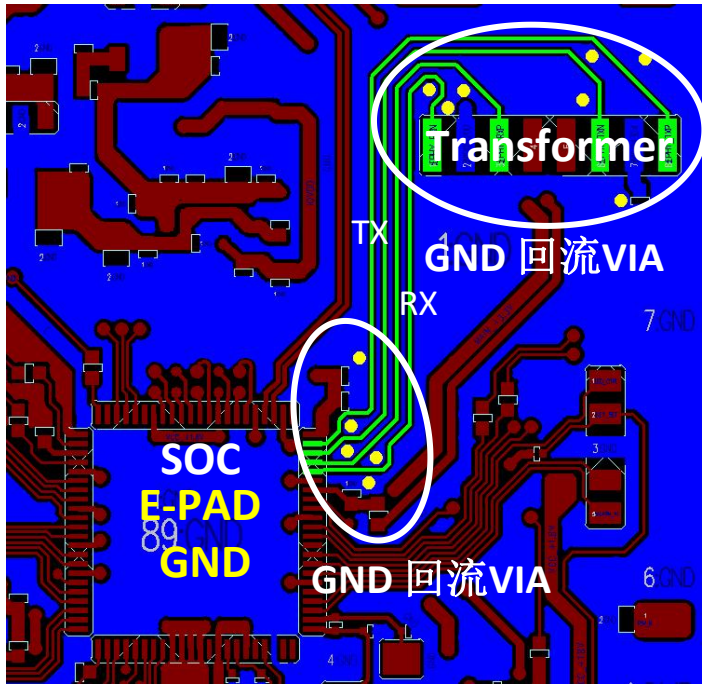
QFN – 4L-PCB - EPHY Routing –表层走线– 线长>40mm

Signal	Layer	Zo	Trace width/spacing (mm)	Shielding Rule
EPHY TX/RX P/N rout	Top	No control	0.125/0.125/0.125 (Ws/Sg/Wg)	(1) P/N 之间须有GND trace shielding (2) TX/RX 之间须有GND trace shielding (3) GND trace VIA rule: 1) 需确认靠近SOC端的GND trace 至少有一颗VIA与SOC PKG E-pad构成回路 2) 需确认靠近transformer端的GND trace至少有一颗VIA与transformer GND pin构成回路

EPHY TX/RX



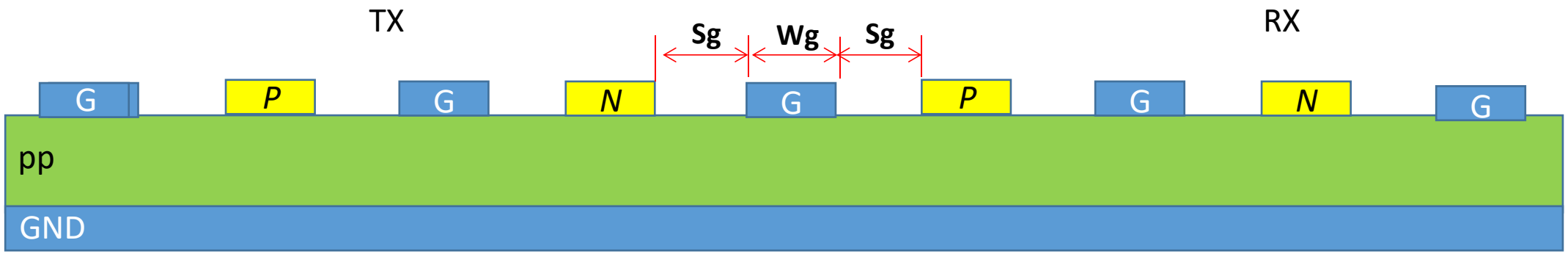
Shielding GND VIA



QFN 4L-PCB EPHY Routing –表层走线– 线长>40mm

Signal	Layer	Requirement	Layout Rule
EPHY TX/RX	Top	TX to RX GND shielding 0.125/0.125 (Wg/Sg)	GND trace VIA rule: 1) 需确认靠近SOC端的GND trace 至少有一颗VIA与SOC PKG E-pad构成回路 2) 需确认靠近transformer端的GND trace至少有一颗VIA与transformer GND pin构成回路

EPHY TX/RX Isolation



EPHY Routing – Length Matching Rule

Signal	Matching Reference	Matching Length
EPHY TX/RX Diff pair	P/N intra skew	<=0.5mm (20mils)

Single-end 讯号绕线

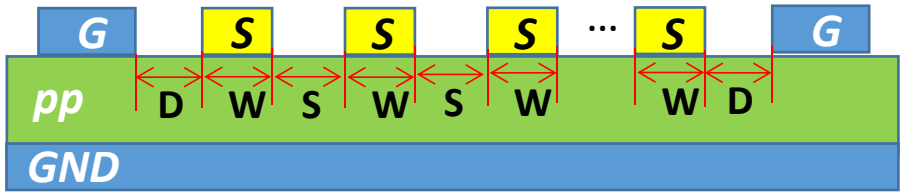
QFN PKG: CV1800B/CV1801B/CV1802B

4-Layer

QFN – 4L-PCB - Single-end – Rule

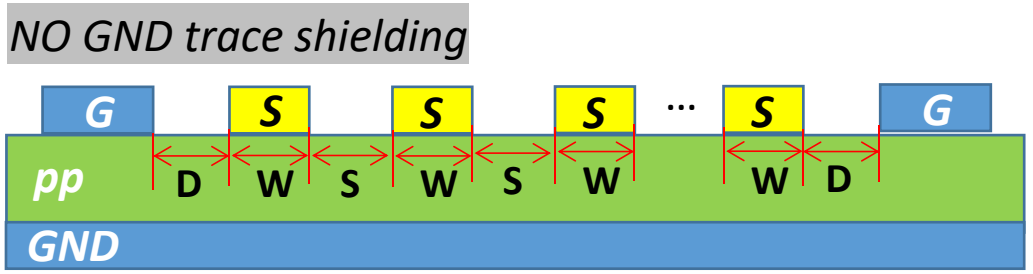
Signal	Layer	Shielding Rule	Trace width/spacing (mm)
SDIO **RTC**	4L-PCB: Top/Bottom	Break out (fan-out) region: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.1/0.1 (S/D) (0.1mm spacing)
		Main rout: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.15/0.1 (S/D) (0.15mm spacing)

NO GND trace shielding



QFN – 4L-PCB – EMMC – Rule

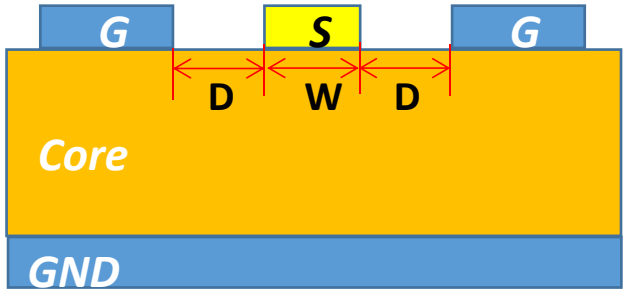
Signal	Layer	Shielding Rule	Trace width/spacing (mm)
NOR/NAND	Top	Break out (fan-out) region: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.1/0.1 (S/D) (0.1mm spacing)
		Main rout: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.15/0.1 (S/D) (0.15mm spacing)



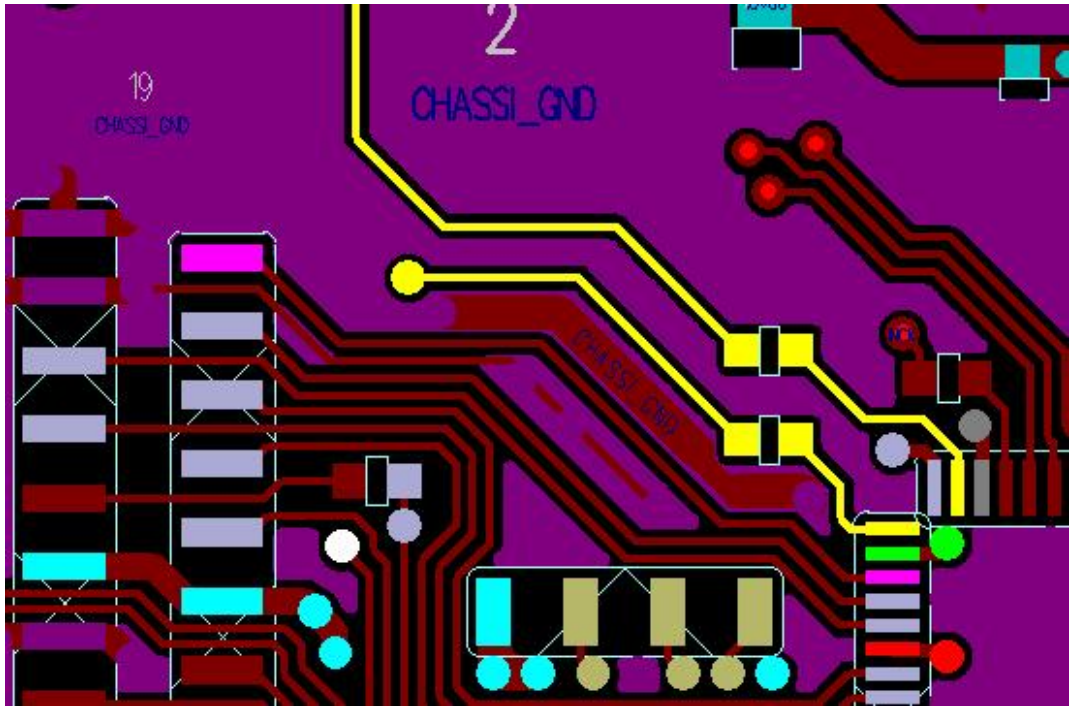
QFN 4L-PCB – AUD – Rule

Signal	Layer	Shielding Rule	Trace width/spacing (mm)
AUD_MIC_L **AADC_AIN_MIC1** **AUD_OUT**	Top	(1) per trace shielding **(2) ref AUD GND plane** **(3) 确认AUD 讯号线下方有完整 GND plane**	(1) W>=0.1 (2) D=0.1

Per trace shielding



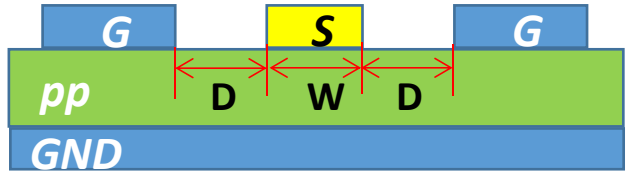
AUD@Top



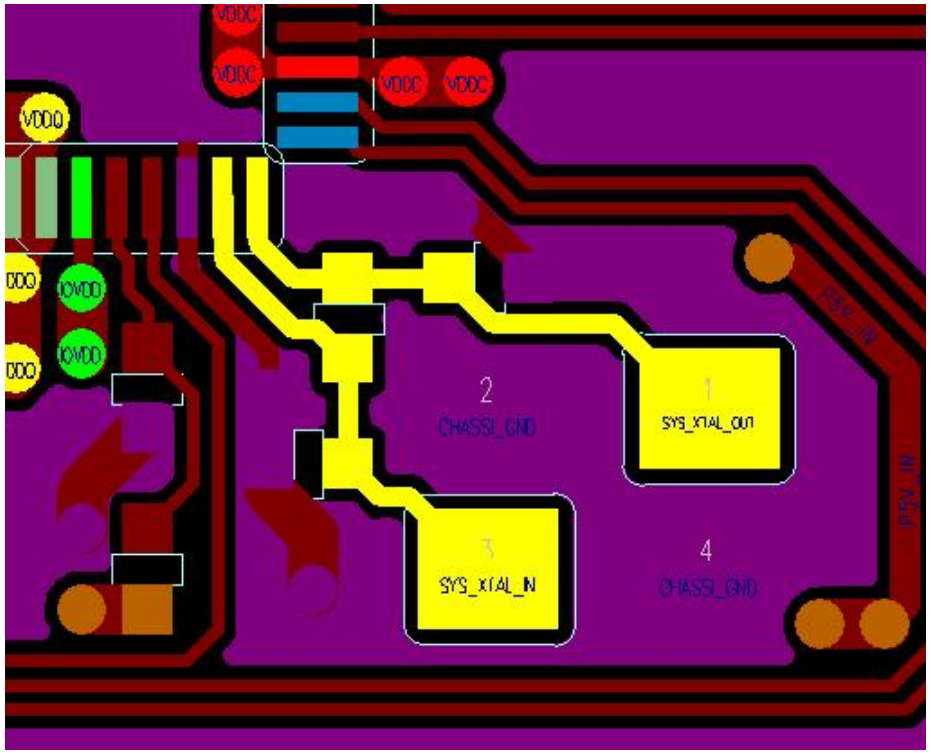
QFN – 4L-PCB – XTAL_IN/OUT - Rule

Signal	Layer	Shielding Rule	Trace width/spacing (mm)
SYS_XTAL_IN **SYS_XTAL_OUT**	Top	**(1) per trace shielding** **(2) ref GND plane**	0.25/0.25 (W/D)

Per trace shielding



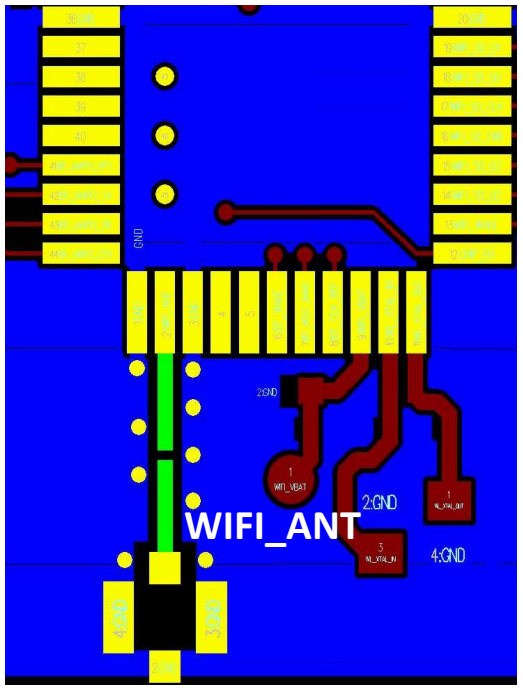
QFN XTAL@Top



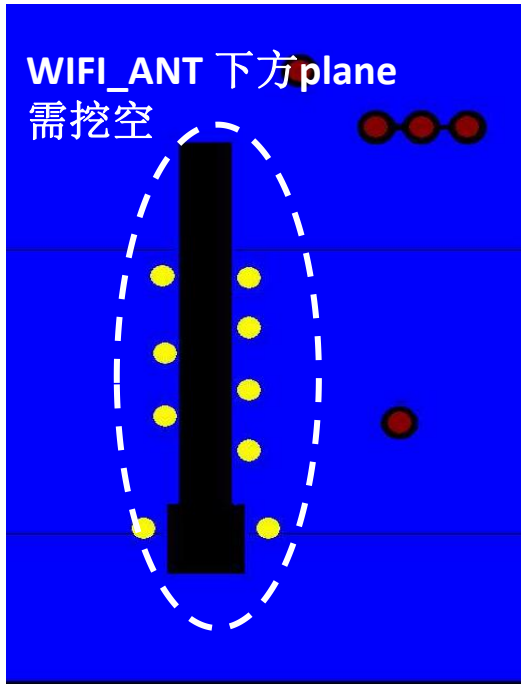
QFN – 4L-PCB – WIFI_ANT Layout Rule

Signal	Layer	Zo	Shielding Rule	Trace width/spacing (mm)
WIFI_ANT	Top	50ohm	Per trace shielding	0.75/0.15/0.3 (W/D1/D2)

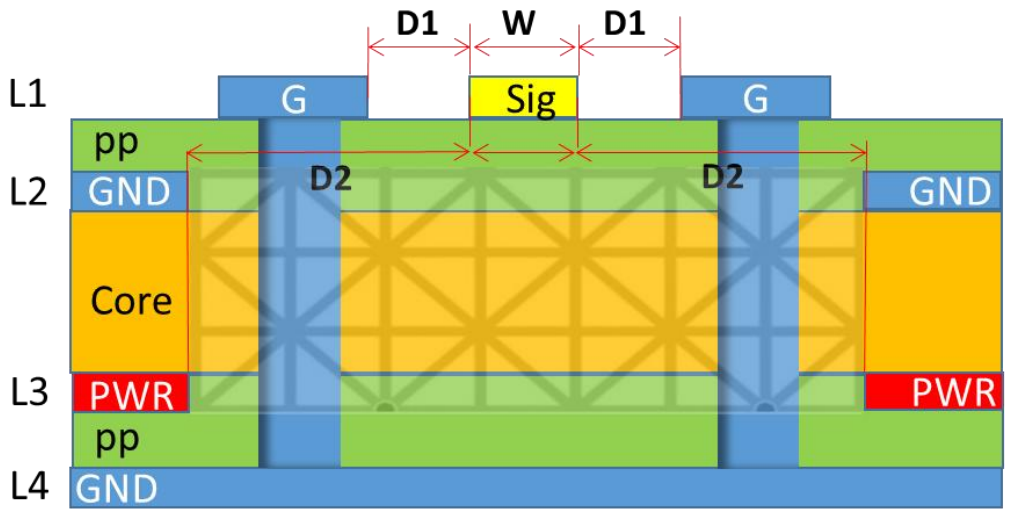
WIFI_ANT@Top



WIFI_ANT@GND/PWR plane



4L-PCB



模拟/数字电源绕线

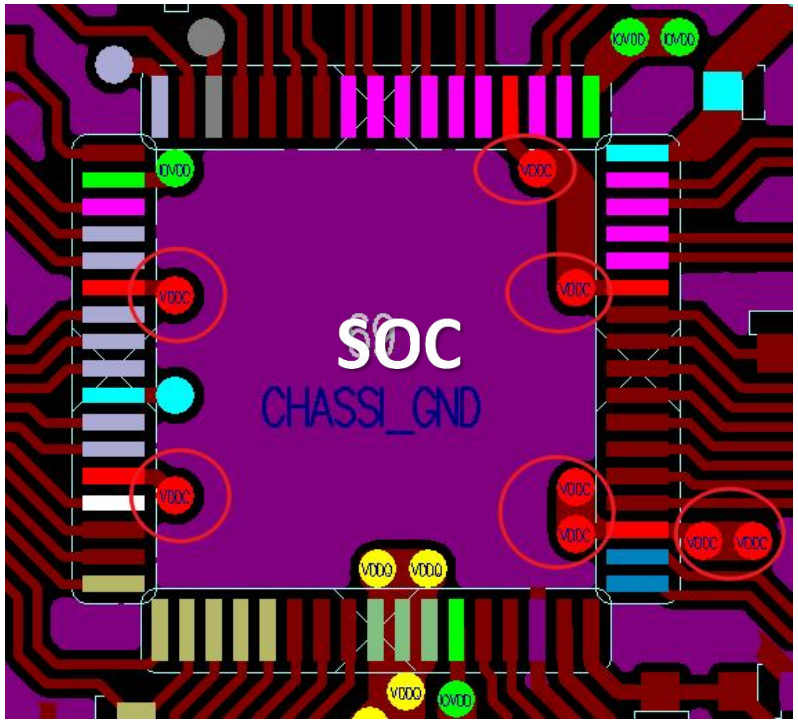
QFN PKG: CV1800B/CV1801B/CV1802B

4-Layer

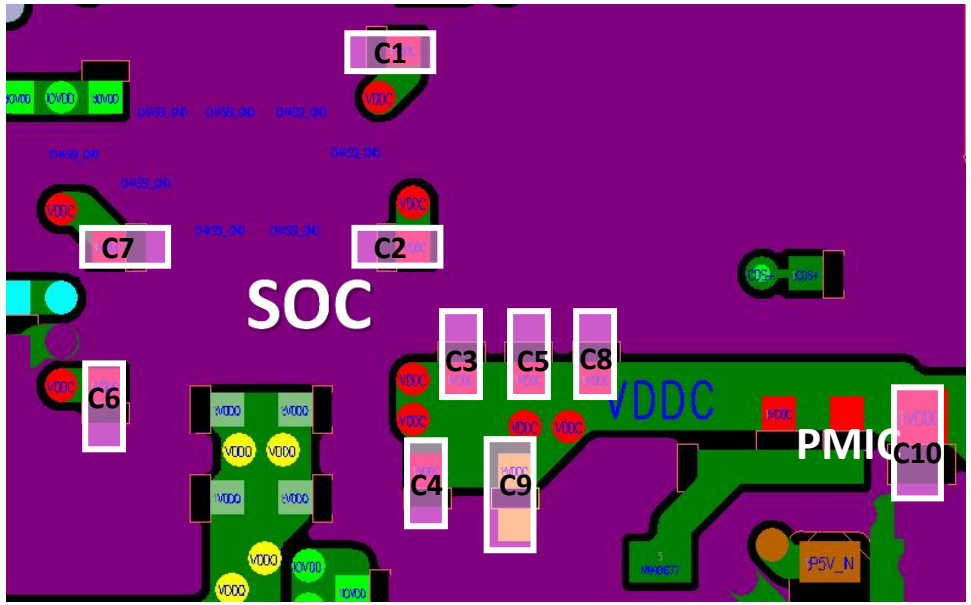
QFN – 4L-PCB – VDDC – Rule 1

Power	Layer	SOC VIA count	DeCap	Layout rule
VDDC	Top/Bottom	5	(1) 0402 0.1uF: C6/C7/C8/C9 (2) 0402 1uF: C1/C3/C5 (3) 0402 4.7uF: C2/C4 (4) 0603 10uF: C10	(1) VDDC VIA rule 每根VDDC pin 需连接1颗VIA (2) GND VIA rule **确认每颗Cap旁至少1颗GND via**

VDDC@Top



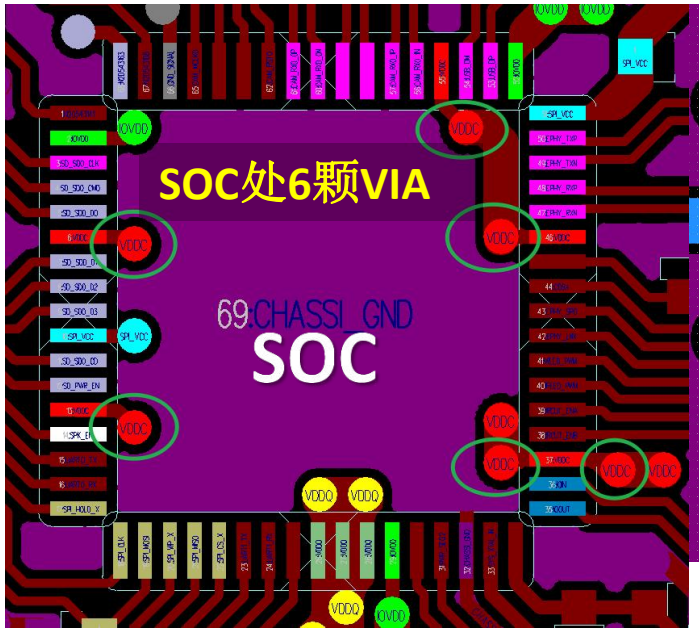
VDDC@Bottom



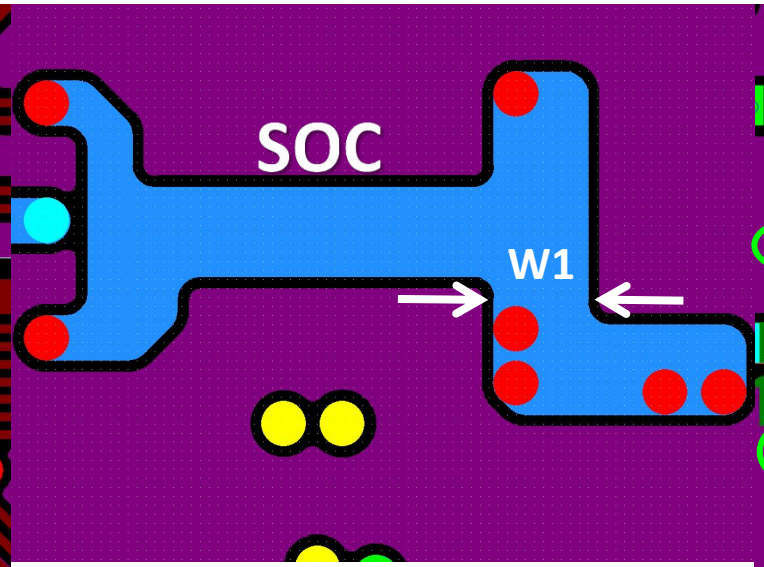
QFN – 4L-PCB - VDDC – Rule 2

Power	Layer	Layout rule
VDDC	L3/Bottom	DDR3_1.35V 内层绕线; (1) 确认SOC处5颗VIA (2) **SOC区域尺寸:** **1) SOC QFN正下方,扣除破孔有效宽度: W1>=1mm** 2) L1<=10mm,扣除破孔有效宽度: W2>=1.0mm **(进入SOC 区域, 板形<=38x38mm2)** 3) L1>10mm,扣除破孔有效宽度: W2>=1.5mm **(进入SOC 区域, 板形>38x38mm2)**

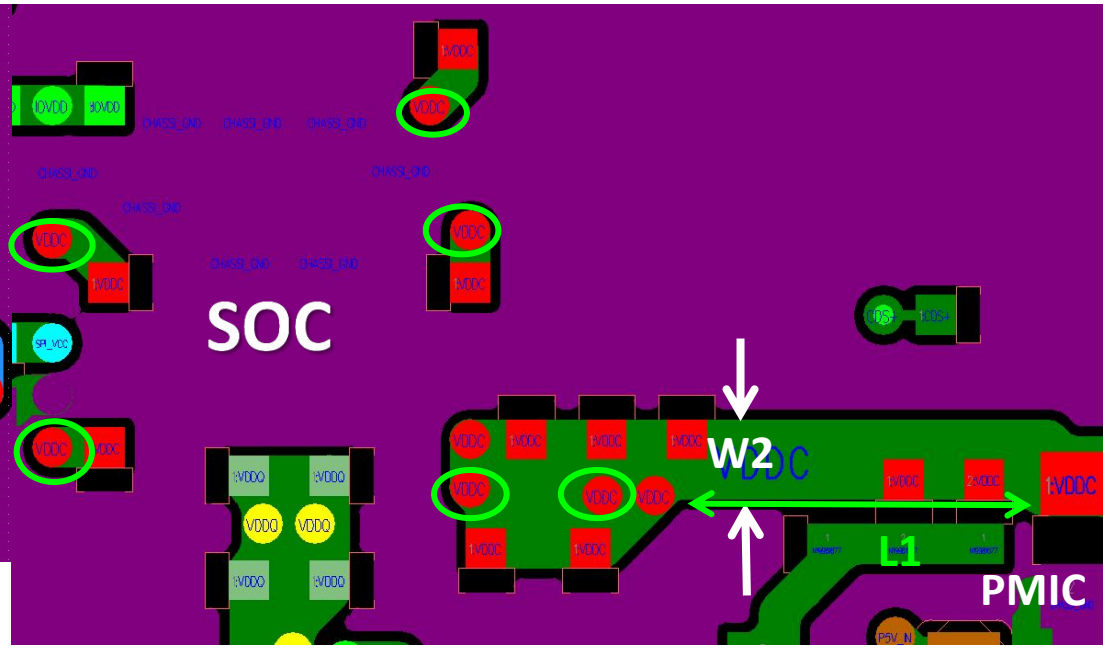
VDDC@Top



VDDC@L3



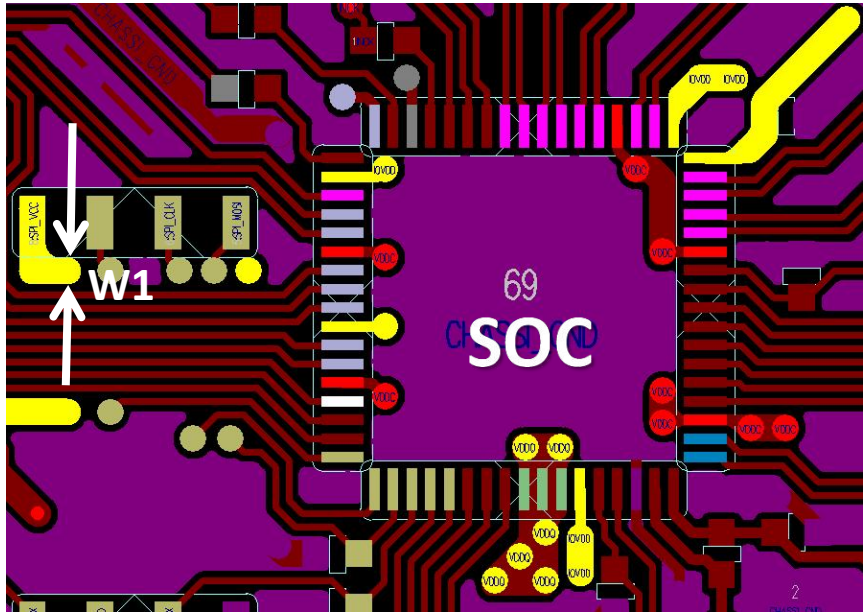
VDDC@Bottom



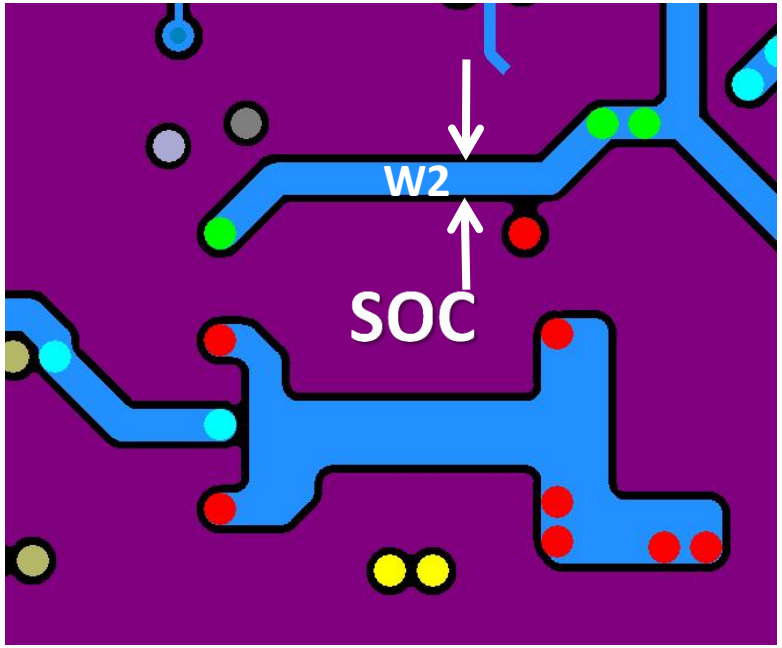
QFN – 4L-PCB – Analog IO Power – Rule 1

Power	Layer	Layout rule
VDDC_+1.8V **Main_+3.3V**	L1/L3/L4	@Top: (1)SoC以外:线宽 W1>=0.5mm @L3/Bottom:所有线宽 W2>=0.5mm

Analog IO power@Top



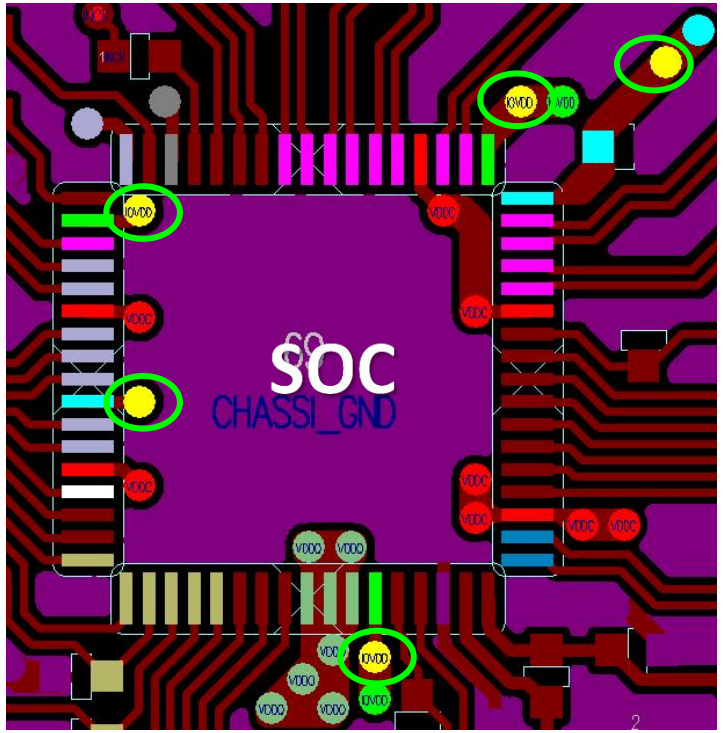
Analog IO power@内层



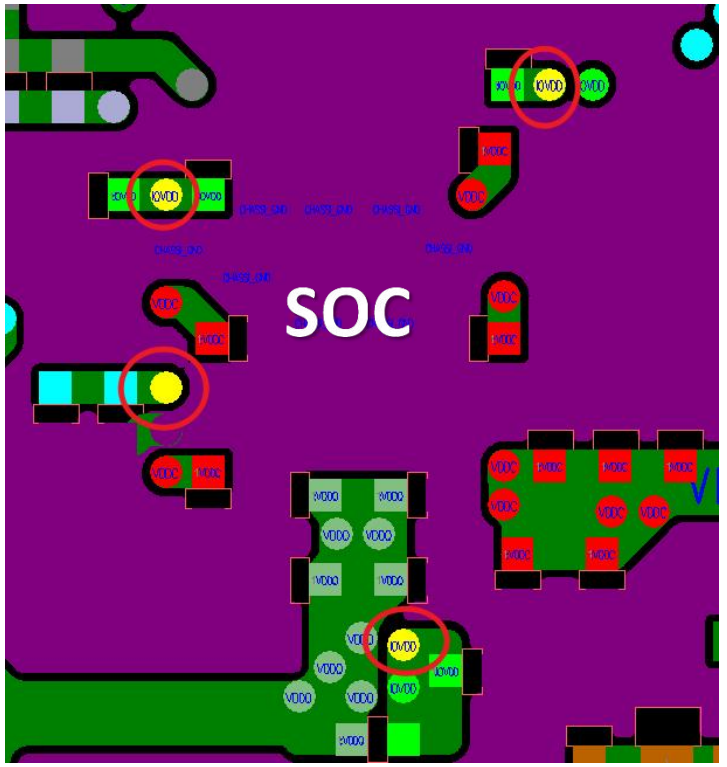
QFN – 4L-PCB - Analog IO Power – Rule 2

Power	Layer	Layout rule
VDDC_+1.8V **Main_+3.3V**	L1/L3/L4	(1) Analog IO power VIA rule 每根VDDC pin 需连接1颗VIA (2) GND VIA rule 确认每颗Cap旁至少1颗GND via

Analog IO power@Top



Analog IO power@Bottom



Appendix

MIPI/EPHY/USB/Antenna 阻抗控制

4-layer PCB

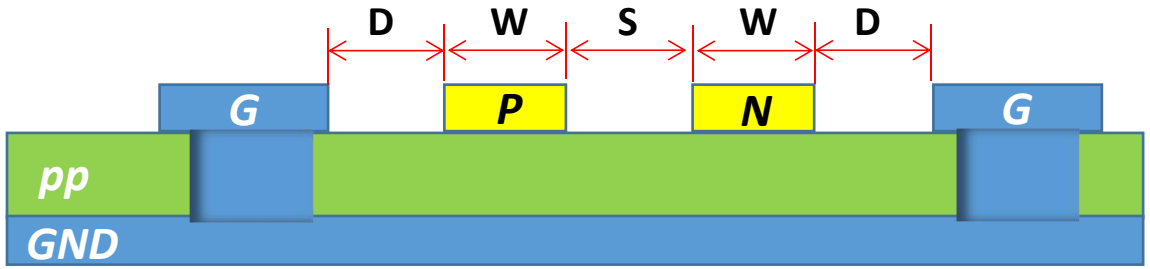
MIPI/EPHY/USB 阻抗控制 –表层走线 Option1

Layer	Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
Top/Bottom	100	5	5	6	97.99
	90	5	4	6	92.48

Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

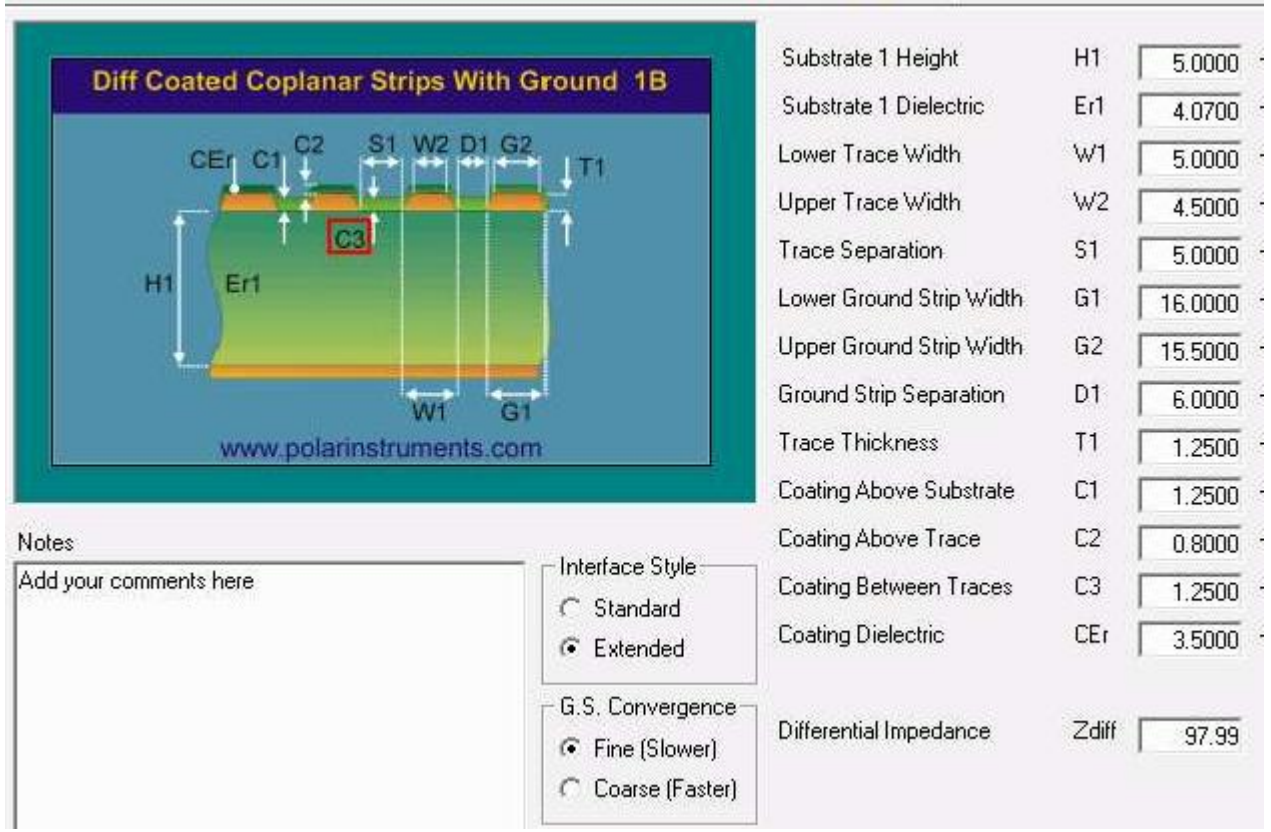
- MIPI/USB differential signals are required impedance control
  - Target impedance:
  (1) MIPI- CSI/DSI: 100ohm
  (2)USB: 90ohm

- Differential signals shielding rule:
  - pair to pair GND shielding

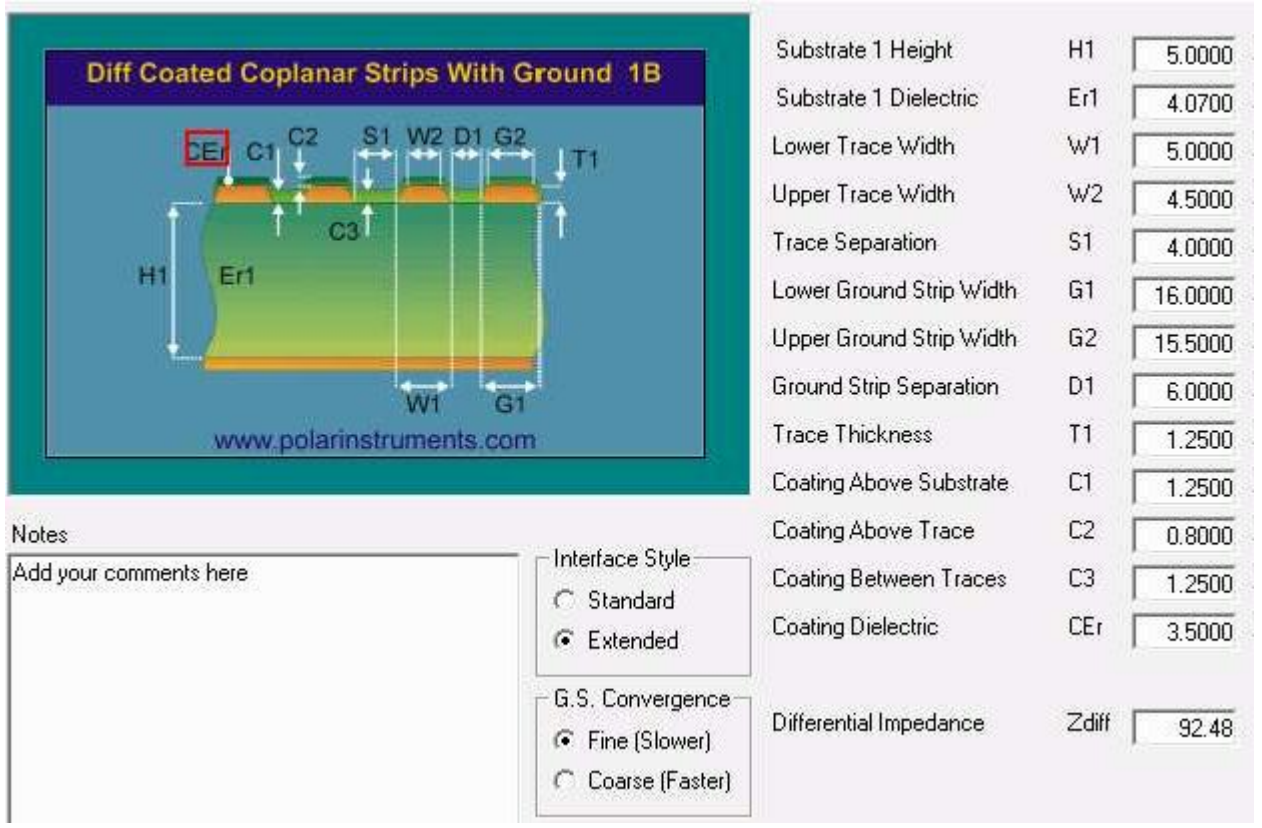


MIPI/EPHY/USB 阻抗控制 –表层走线 Option1

Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
100 +/- 5%	5	5	6	97.99



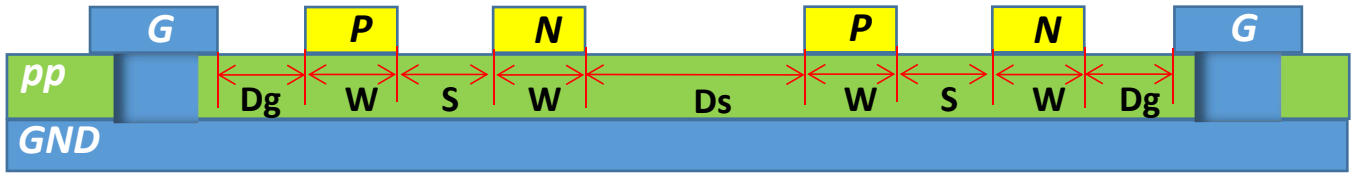
Target Z	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
90 +/- 5%	5	4	6	92.48



MIPI 阻抗控制 – 表层走线 Option2

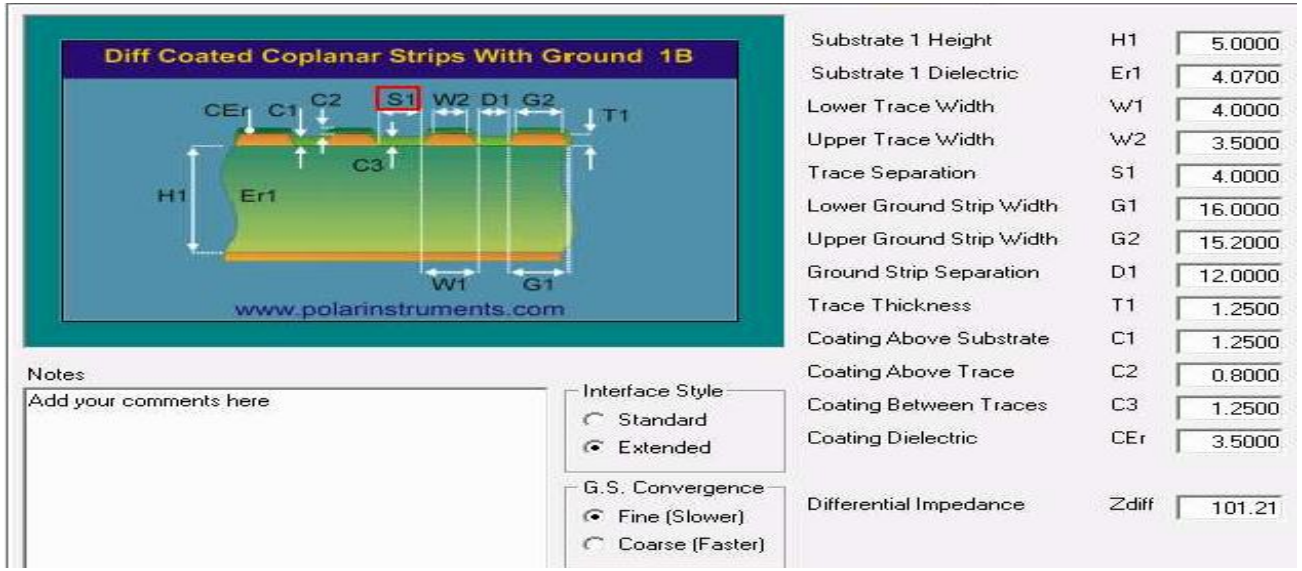
Layer	Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)	Rule
Top/Bottom	100	5	5	12	12	99.96	Ds=3W, Dg=3W

Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

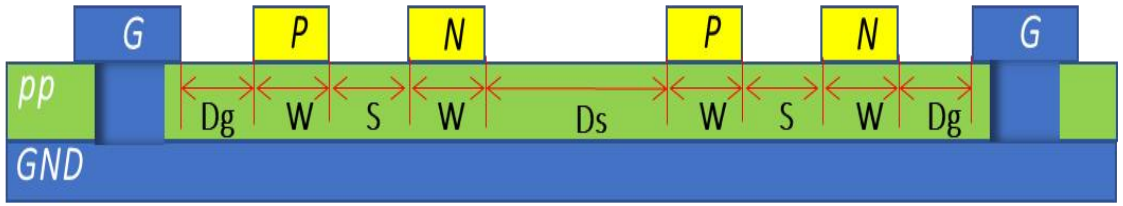


MIPI 阻抗控制 – 表层走线 Option2

Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
100 +/- 5%	5	5	12	12	99.96
	4	4	12	12	101.21



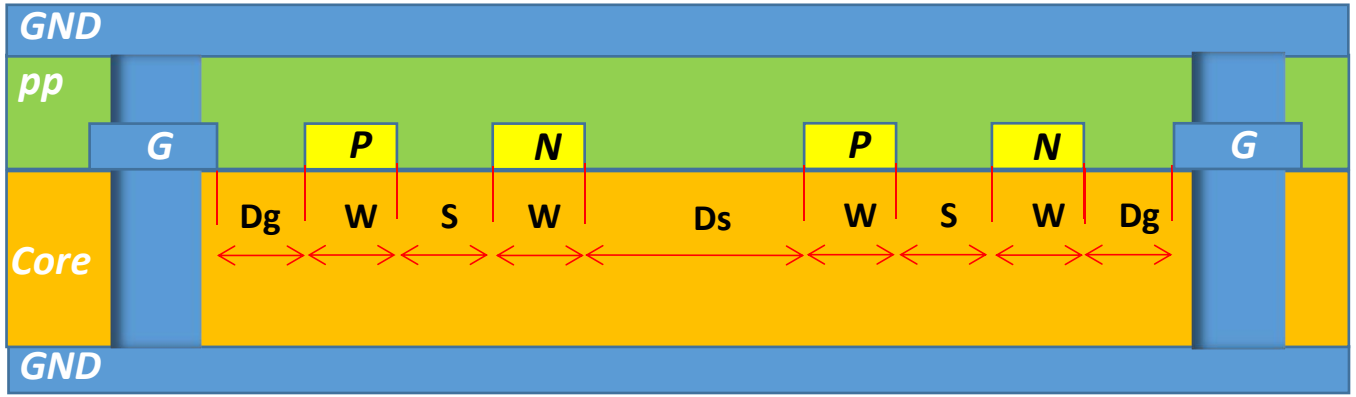
Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	



MIPI 阻抗控制 – 内层走线

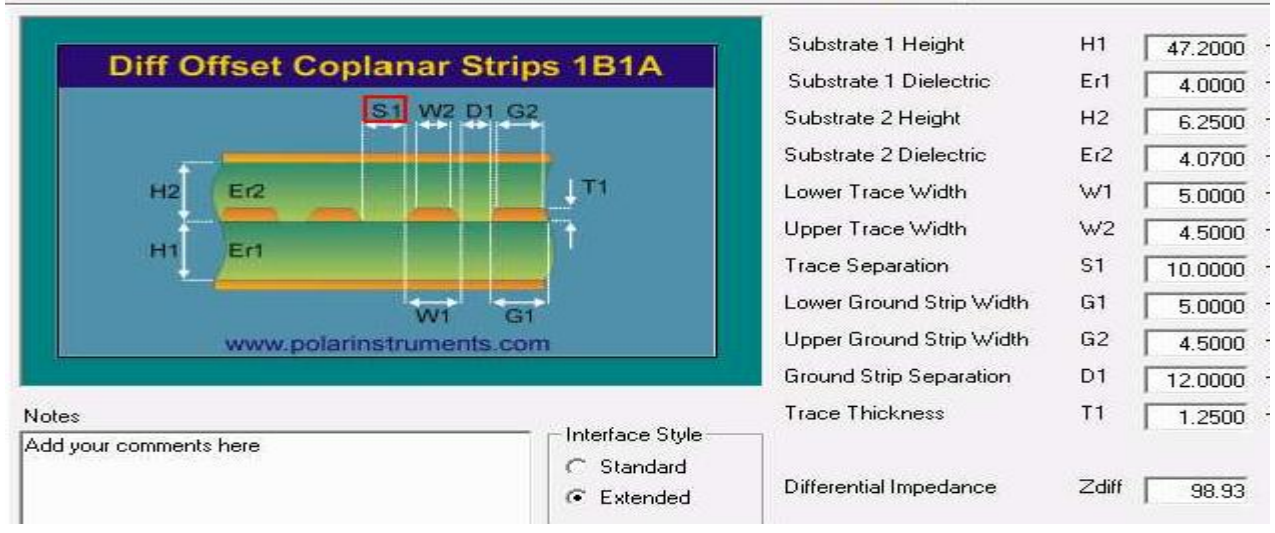
Layer	Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
L2/L3	100	5	10	12	12	98.93

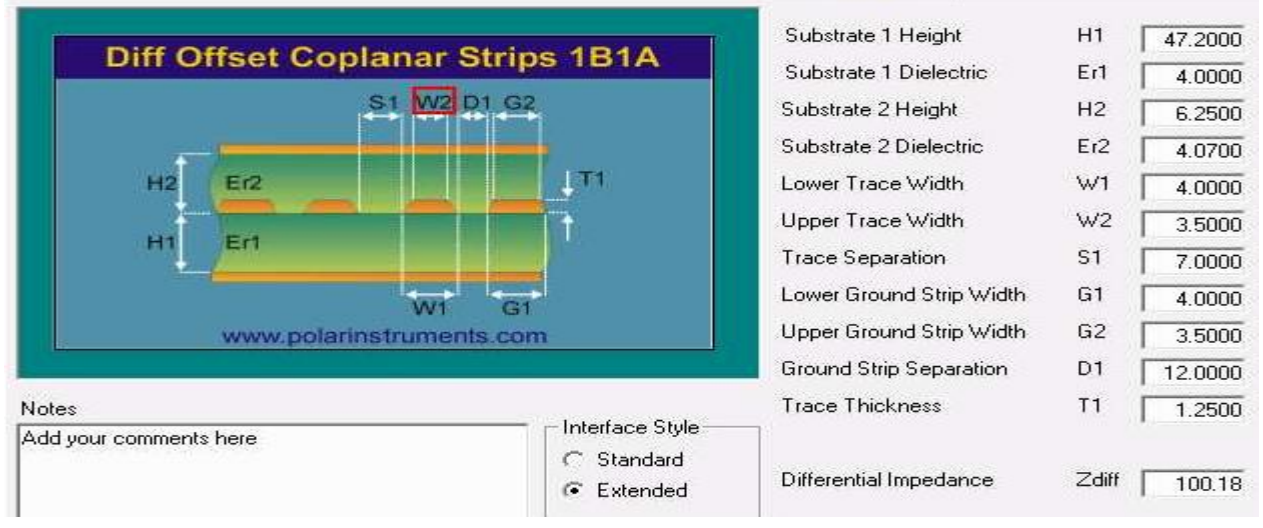
Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	



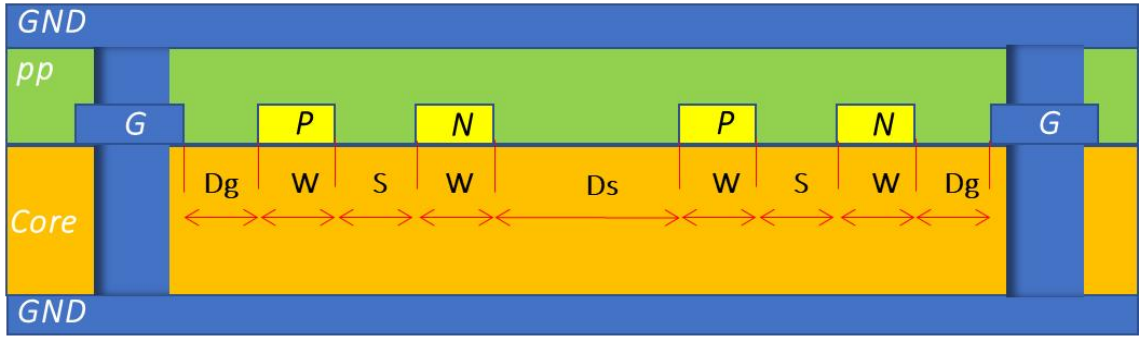
MIPI 阻抗控制 – 内层走线

Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
100 +/- 5%	5	10	12	12	98.93
	4	7	12	12	100.18





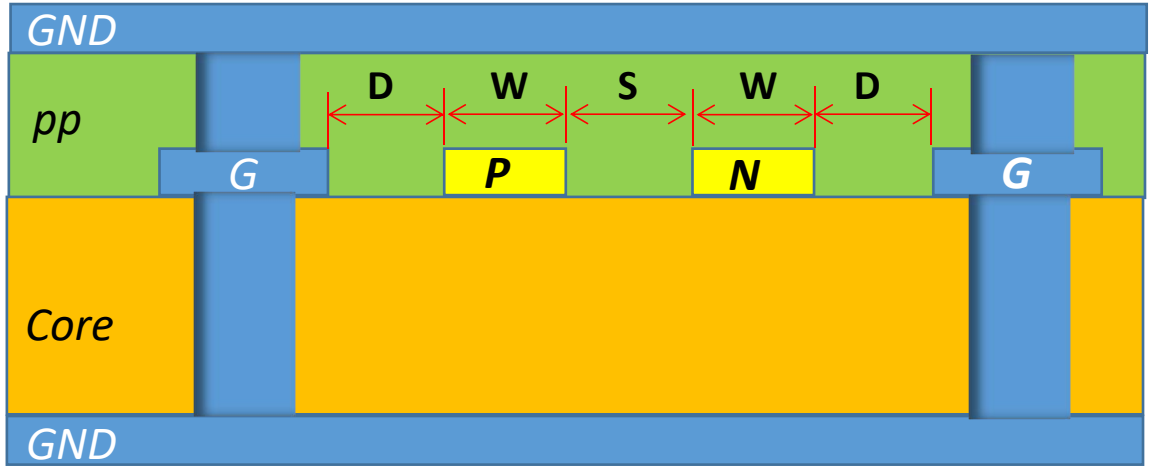
Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	



EPHY/USB 阻抗控制 – 内层走线

Layer	Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
L2/L3	100	5	10	12	98.92
	90	5	7	6	90.33

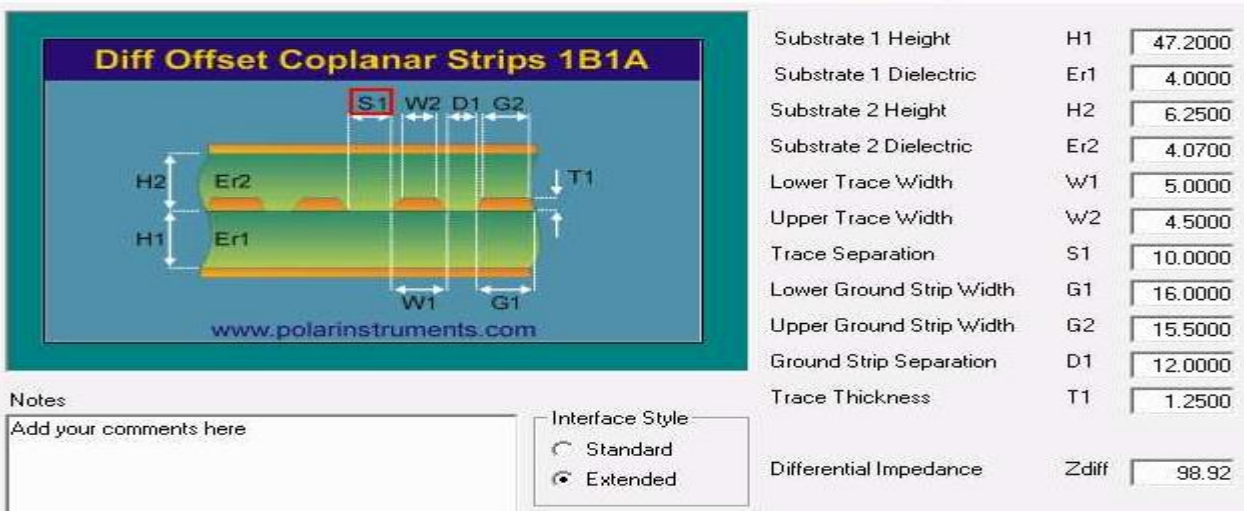
Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

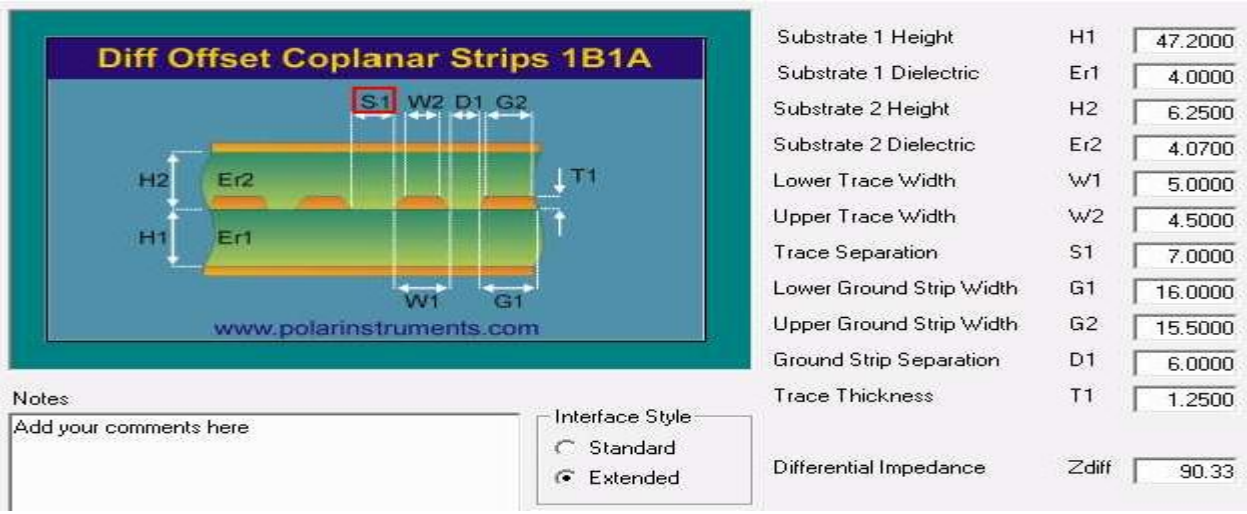


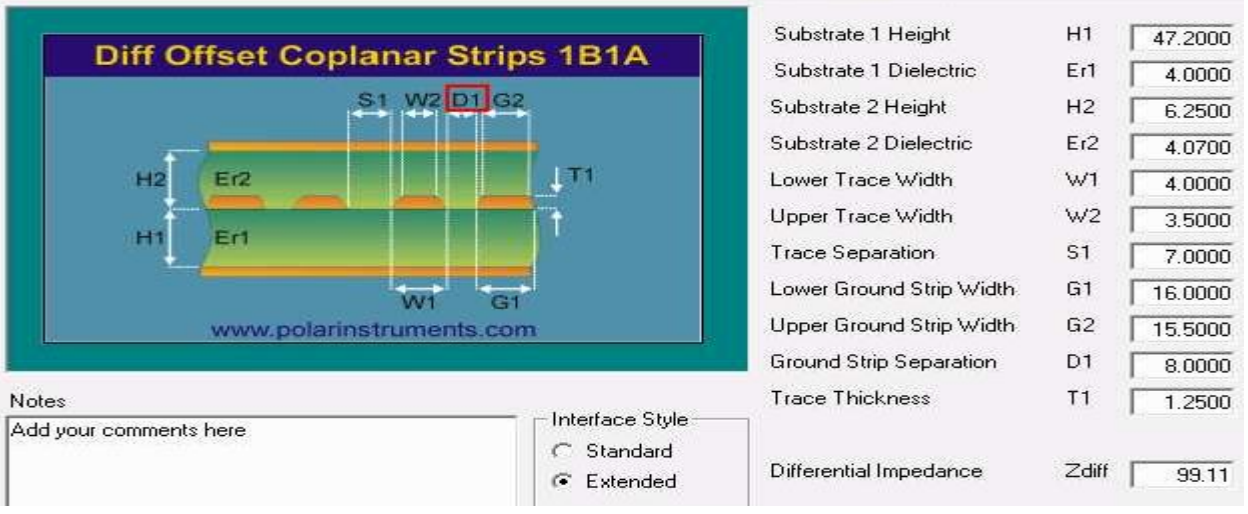
EPHY/USB 阻抗控制 – 内层走线

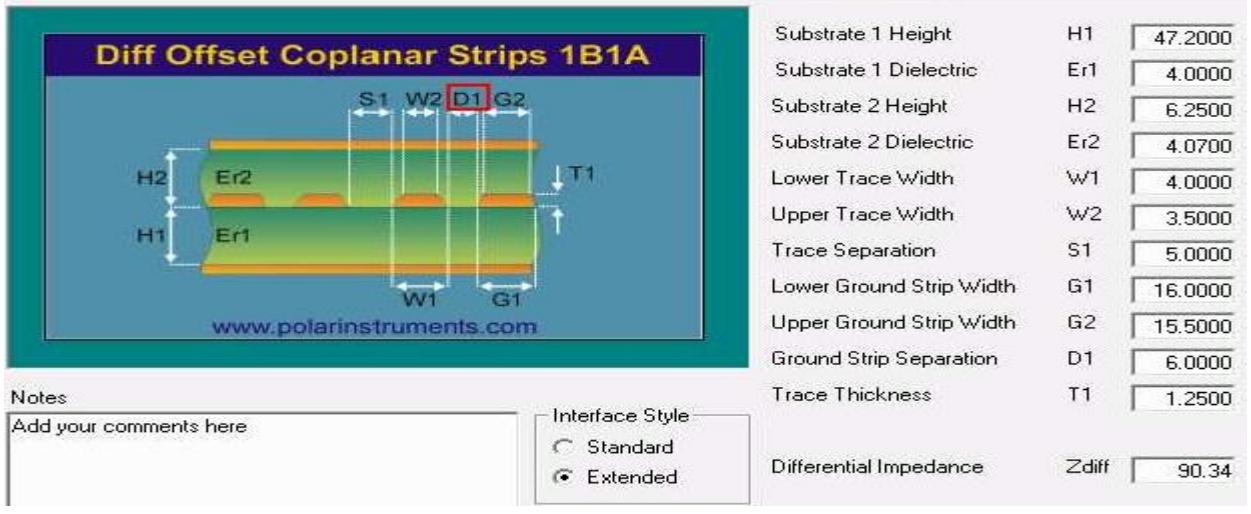
Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
100 +/- 5%	5	10	12	98.92
	4	7	8	99.11

Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
90 +/- 5%	5	7	6	90.33
	4	5	6	90.34





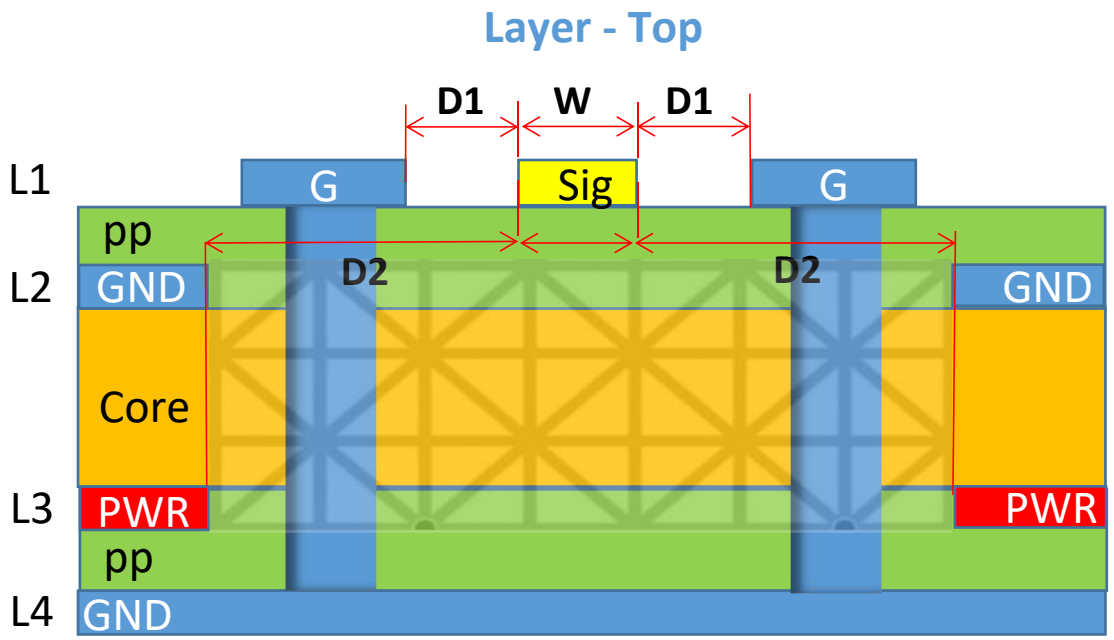




Antenna 50ohm 阻抗控制

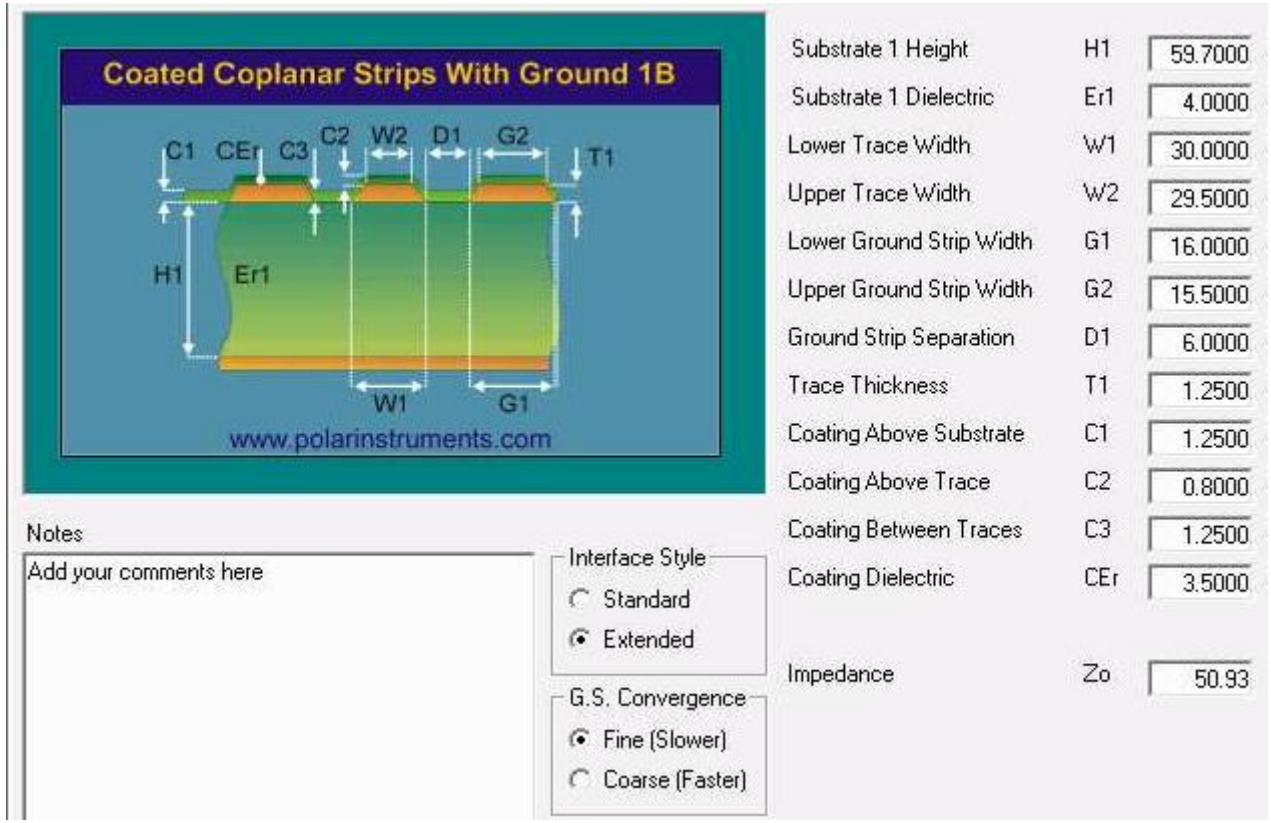
Layer	Target Z (ohm)	W (mils)	D1 (mils)	D2(mils)	Estimated Z (ohm)	Note
Top	50	30	6	12	50.93	Ref layer L4

Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	



Antenna 50ohm 阻抗控制

Target Z (ohm)	W (mils)	D1 (mils)	D2(mils)	Estimated Z (ohm)
50 +/- 5%	30	6	12	50.93



Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8